Unit 8.

Combinational Circuit Design and Simulation Using Gates

Outline

- ✓ Review of Combinational Circuit Design
- ✓ Design of Circuits with Limited Gate Fan-In
- ✓ Gate Delay and Timing Diagrams
- ✓ Hazards in Combinational Logic
- ✓ Simulation and Testing of Logic Circuits

8-1 Review of Combinational Circuit Design

- ✓ **Design of a combinational switching circuit**
  - Setup a truth table which specifies the output(s) as a function of the input variables
  - Derive simplified algebraic expressions for the output functions using K-maps, the Q-M method, or other similar procedures.
- ✓ **Multi-level & Multi-output circuit**
- ✓ **Minimum SOP's starting point**
  - Minimum two-level AND-OR、NAND-NAND、OR-NAND、NOR-OR
- ✓ **Minimum POS's starting point**
  - Minimum two-level OR-AND、NOR-NOR、AND-NOR、NAND-AND

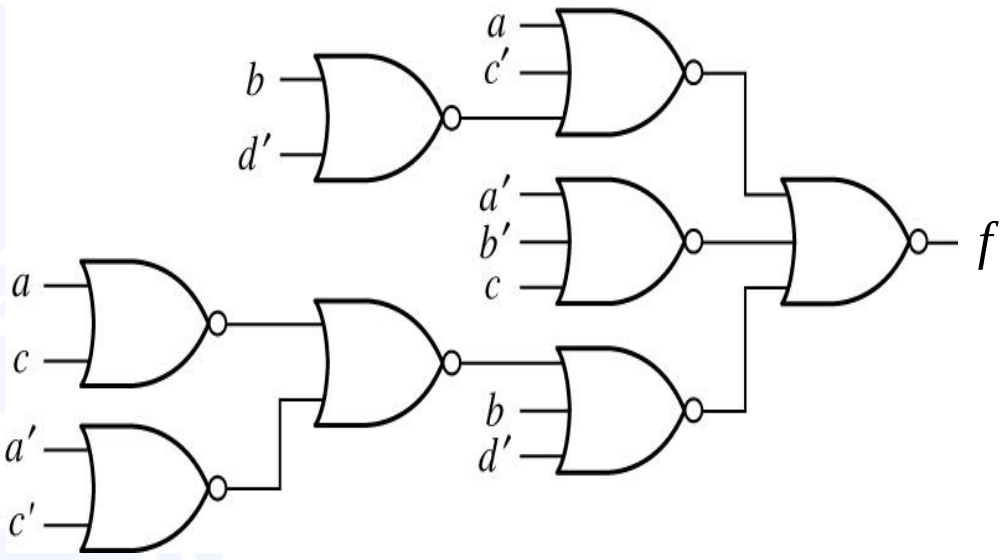
8-2 Circuit with Limited Gate Fan-In

- ✓ **Example I**

  Realize $f(a,b,c,d)=\sum m(0,3,4,5,8,9,10,14,15)$

  using 3-input NOR gates

ab \ cd	00	01	11	10
00	1	1	0	1
01	0	1	0	1
11	1	0	1	0
10	0	0	1	1

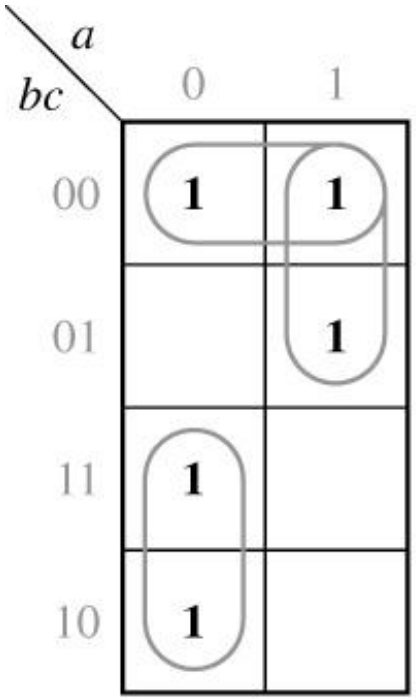


$$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$$

$$= b'd(a'c' + ac) + a'c(b + d') + abc'$$

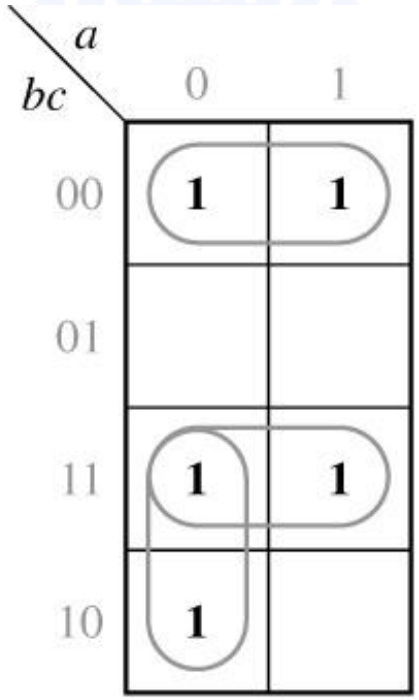
✓ Example II

only using 2-input NAND gates and inverters



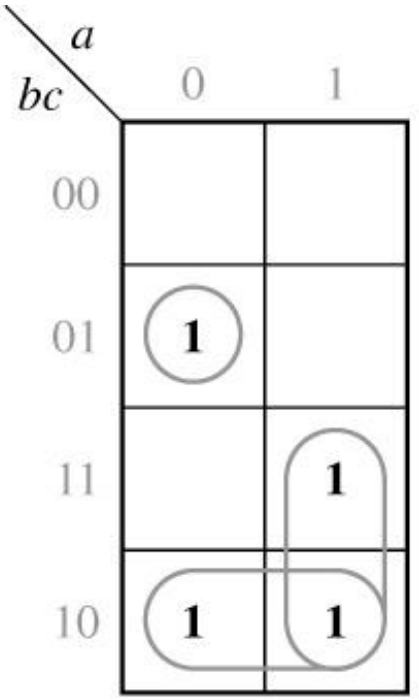
$f_1 = \Sigma m\,(0, 2, 3, 4, 5)$

$$f_1 = b'c' + ab' + a'b$$



$f_2 = \Sigma m\,(0, 2, 3, 4, 7)$

$$f_2 = b'c' + bc + a'b$$



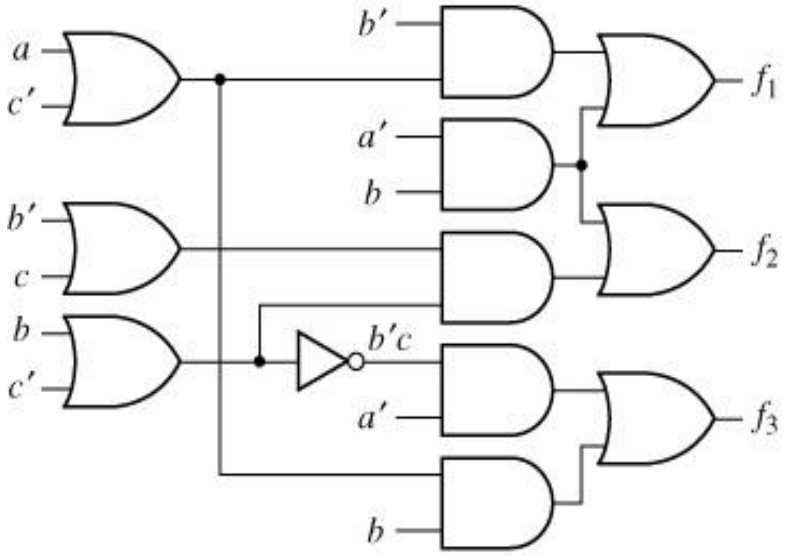
$f_3 = \Sigma m\,(1, 2, 6, 7)$

$$f_2 = a'b'c + ab + bc'$$

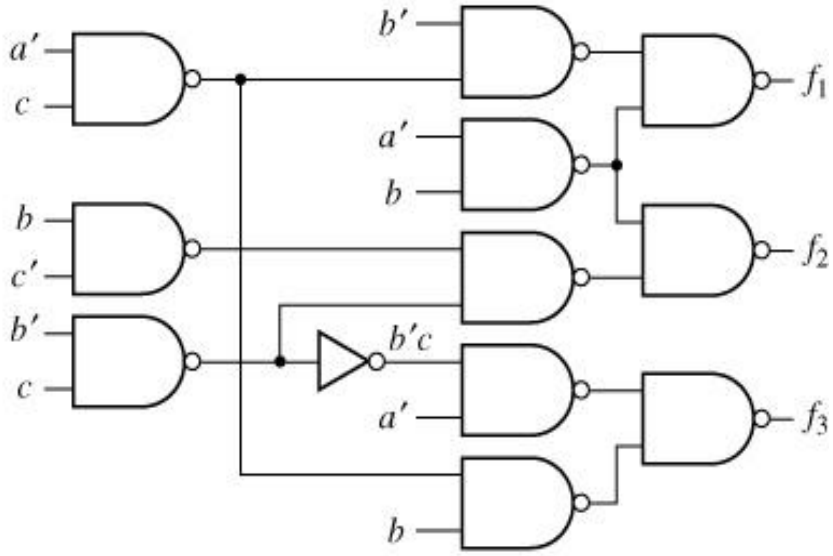
$$f_1 = b'(a + c') + a'b$$

$$f_2 = b(a'+c) + b'c' \quad \text{or} \quad f_2 = (b'+c)(b + c') + a'b$$

$$f_3 = a'b'c + b(a + c')$$

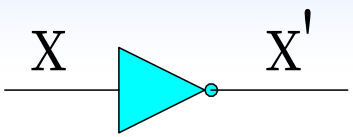


(a)

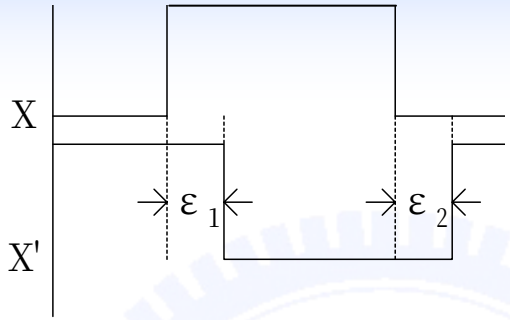


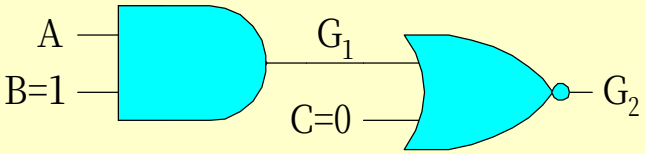
(b)

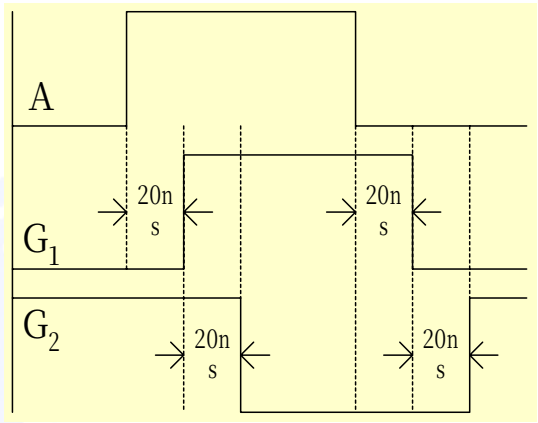
8-3 Gate Delay and Timing Diagrams

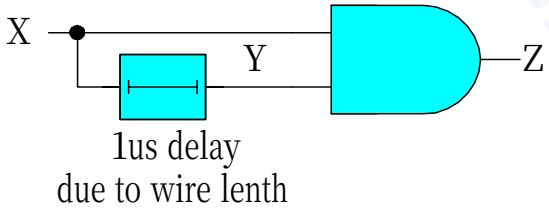


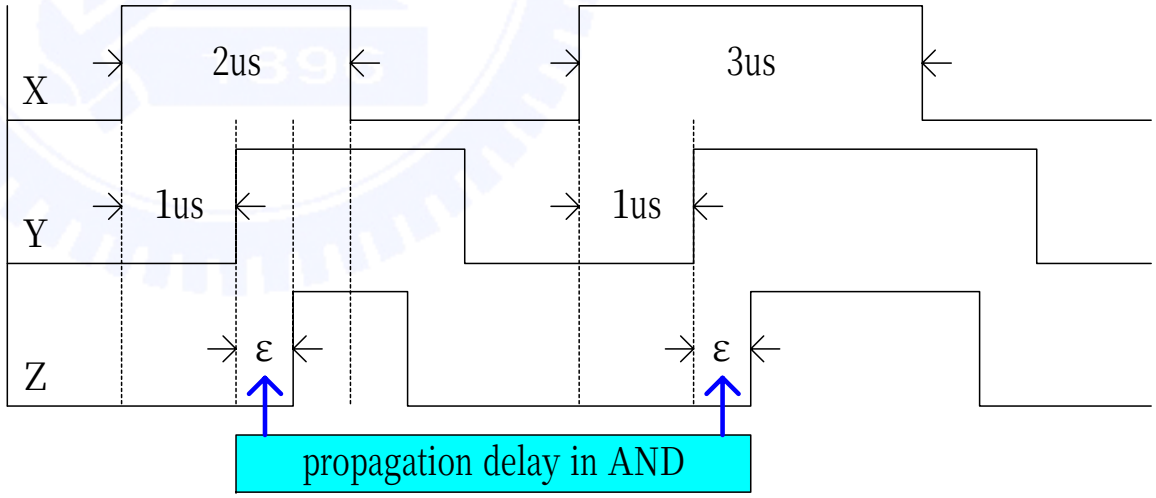
ε_1, ε_2 may be very small but still exist.











8-4 Hazard in Combinational Logic

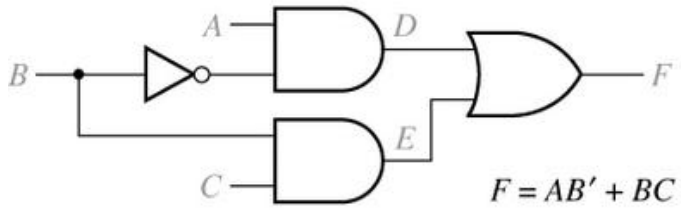
- ✓ **What is hazard?**
  - **Unwanted** switching transients appearing in the output while the input to a combinational circuit changes
- ✓ **Types of hazards**

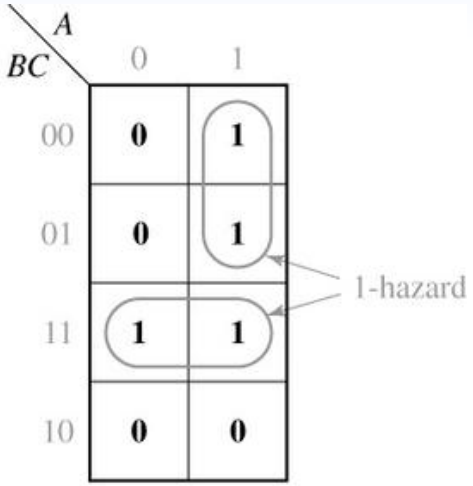
(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazards

- ✓ **In K-Map,**
  - If any two adjacent 1's are not covered by the same loop, a 1-hazard exists for the transition between the two 1's.

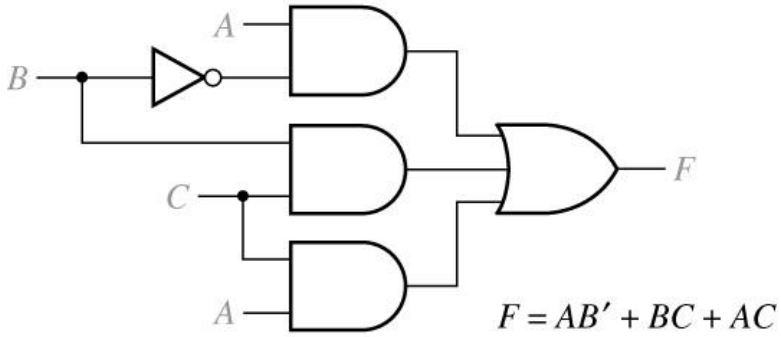
Static 1-hazard

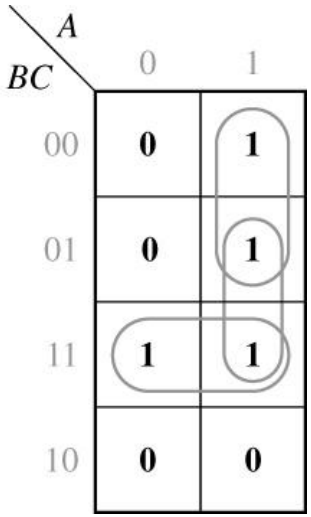
✓ **Let A=1 and C=1**





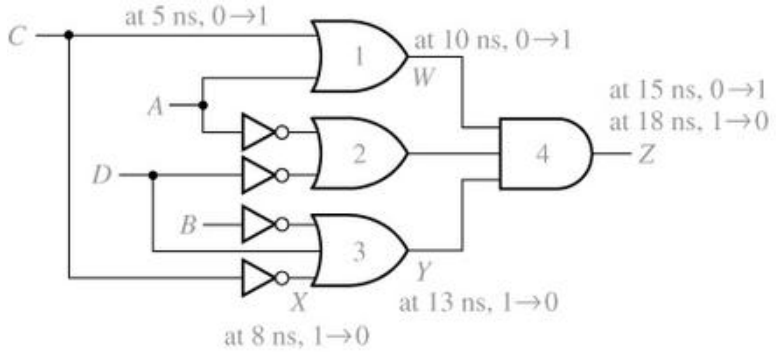
Circuit with Hazard Removed

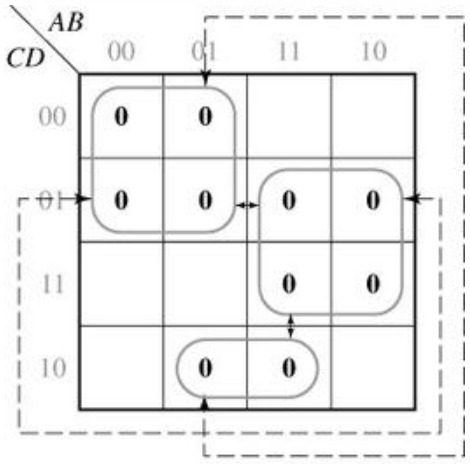




Static 0-hazard

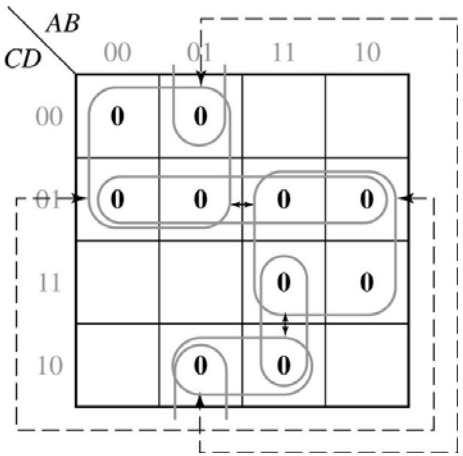
✓ **Let A=0, B=1, and D=0**





Circuit with Hazard Removed

$$F = (A + C)(A'+D')(B'+C'+D)$$



$$F = (A + C)(A'+D')(B'+C'+D)(C + D')(A + B'+D)(A'+B'+C')$$

8-5 Simulation and Testing of Logic Circuits

- ✓ **For simulation logic circuits**
  - Specify the circuit components and connections
  - Determine the circuit inputs
  - Observe the circuit outputs
- ✓ **4-valued logic simulator**
  - 0 (low)、1 (high)、X (unknow)、Z (high impedance)

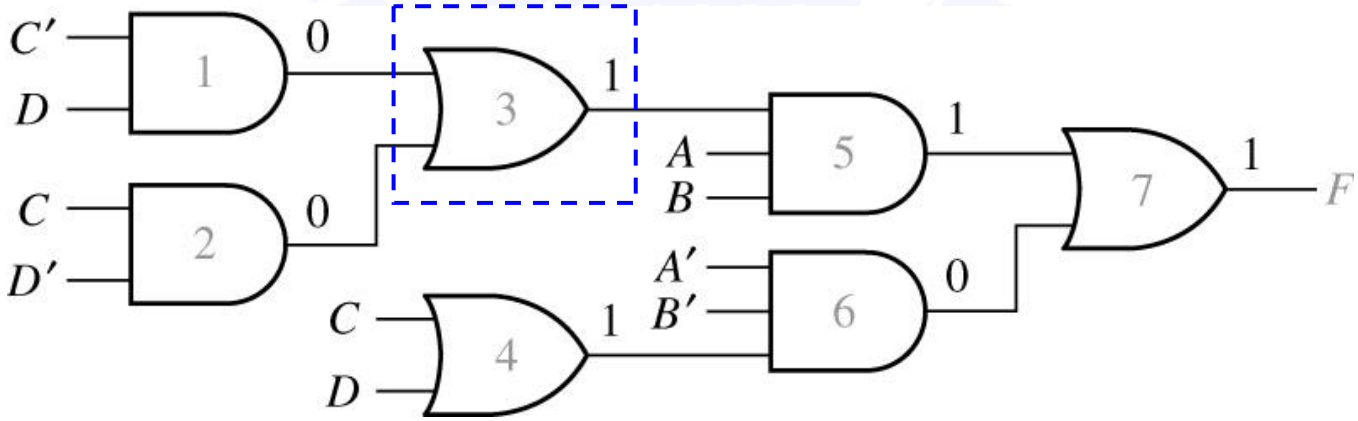
AND & OR function for 4-valued simulation

●	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Testing of logic circuits

- ✓ **In the logic circuit, a wrong output may be due to**
  - Incorrect design
  - Gates connected wrong
  - Wrong input signals to the circuit
  - Defective gates
  - Defective connecting wires
- ✓ **Logic circuit with incorrect output**



Homework

- ✓ 1、3、5、7、10
- ✓ Design Problems