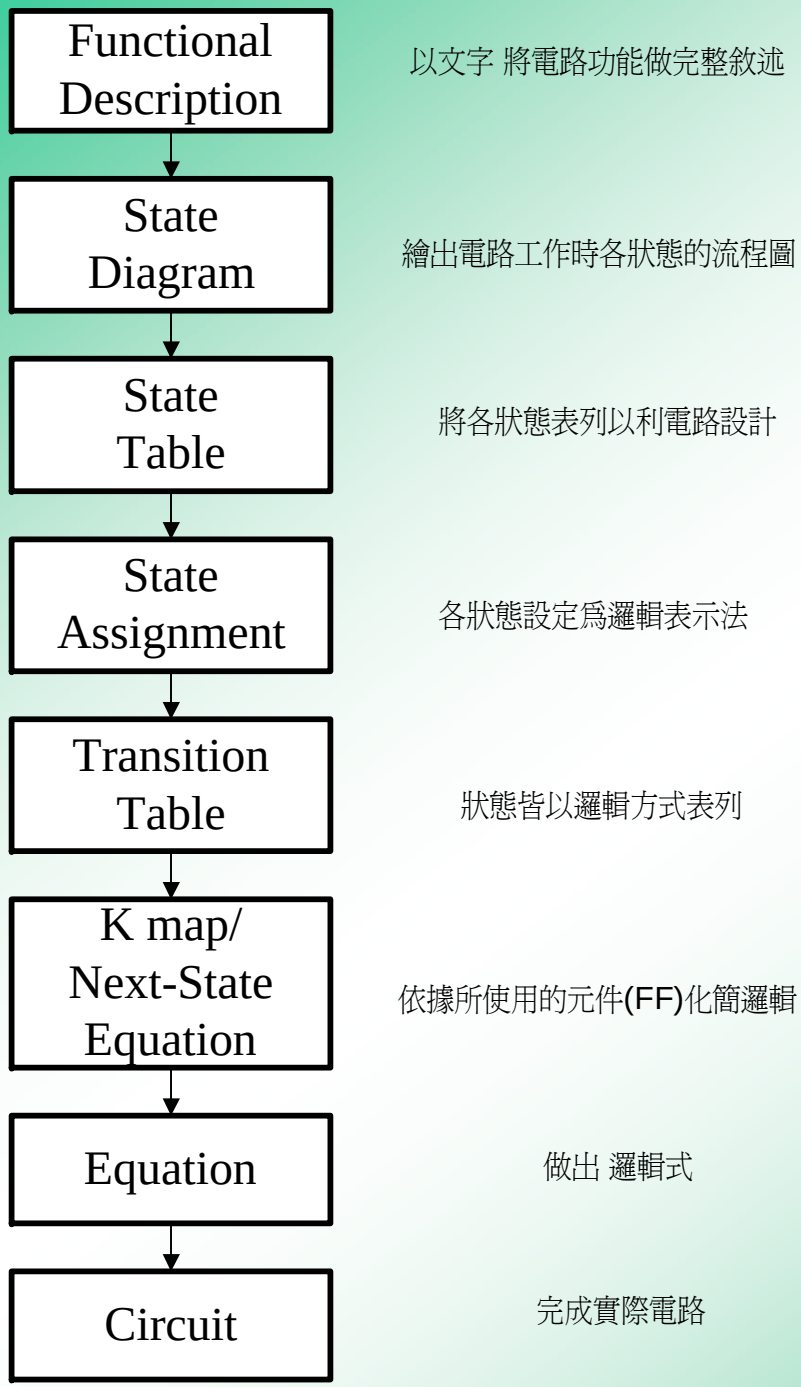
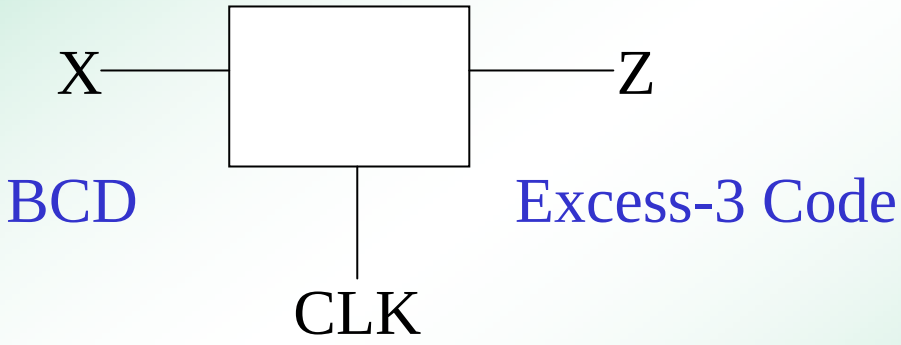
Chap. 16:

Sequential Network Design


Functional Description
以文字 將電路功能做完整敘述
State Diagram
繪出電路工作時各狀態的流程圖
State Table
將各狀態表列以利電路設計
State Assignment
各狀態設定爲邏輯表示法
Transition Table
狀態皆以邏輯方式表列
K map/ Next-State Equation
依據所使用的元件(FF)化簡邏輯
Equation
做出 邏輯式
Circuit
完成實際電路

16 - 2 A Complete Example – Code Converter



X				Z			
t_3	t_2	t_1	t_0	t_3	t_2	t_1	t_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

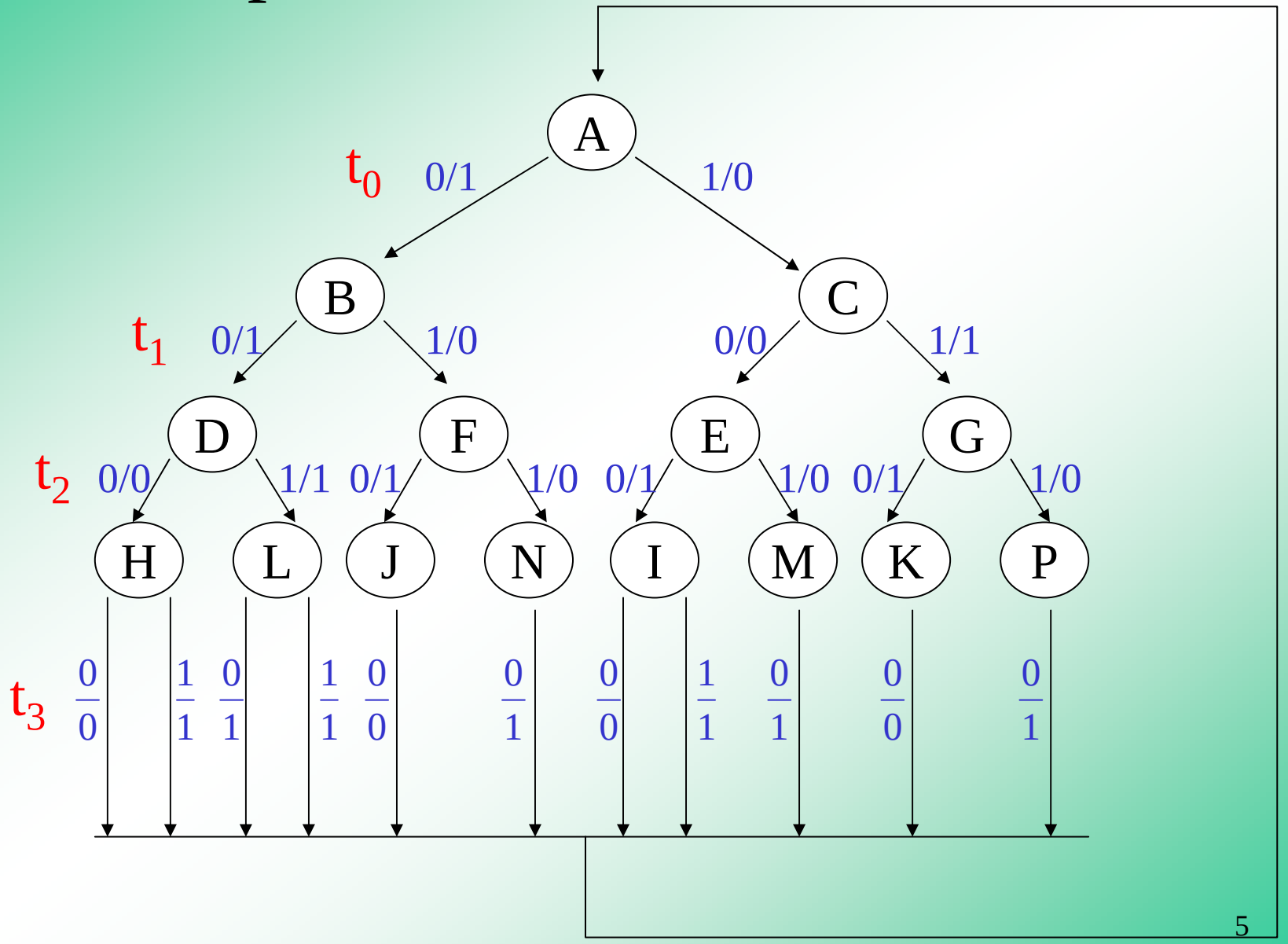
t_0 : $X = \begin{matrix} \boldsymbol{0} \\ \boldsymbol{1} \end{matrix}$ $Z = \begin{matrix} 1 \\ 0 \end{matrix}$

t_1: $X = \begin{matrix} \boldsymbol{0}\{\boldsymbol{0},\ \boldsymbol{1} \\ \boldsymbol{1}\{\boldsymbol{0},\ \boldsymbol{1} \end{matrix}$ $Z = \begin{matrix} \{1,\ 0 \\ \{\boldsymbol{0},\ \boldsymbol{1} \end{matrix}$

t_2 : $X = \begin{matrix} 00\{0,\ 1 \\ 01\{0,\ 1 \\ 10\{0,\ 1 \\ 11\{0,\ 1 \end{matrix}$ $Z = \begin{matrix} \{0,\ 1 \\ \{1,\ 0 \\ \{1,\ 0 \\ \{1,\ 0 \end{matrix}$

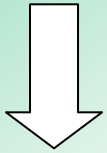
t_3 : $X = \begin{matrix} 000\{0,\ 1 \\ 001\{0,\ 1 \\ 010\{0,\ 1 \\ 011\{0,\ 1 \\ 100\{0,\ 1 \\ 101\{0,\ 1 \\ 110\{0,\ 1 \\ 111\{0,\ 1 \end{matrix}$ $Z = \begin{matrix} \{0,\ 1 \\ \{0,\ 1 \\ \{0,\ - \\ \{0,\ - \\ \{0,\ - \\ \{1,\ - \\ \{1,\ - \\ \{1,\ - \end{matrix}$

State Graph


A
B
C
D
F
E
G
H
L
J
N
I
M
K
P
t_0
t_1
t_2
t_3
0/1
1/0
0/1
1/0
0/0
1/1
0/0
1/1
0/1
1/0
0/1
1/0
0/1
1/0
0/1
1/0
0/0
1/1
0/1
1/0
0/0
1/1
0/1
1/0
0/0
1/1
0/1
1/0

State Table

	P.S.	N.S. x = 0	N.S. x = 1	Z x = 0	Z x = 1
t_0	A	B	C	1	0
t_1	B	D	~~F~~ E	1	0
	C	E	~~G~~ E	0	1
t_2	D	H	~~L~~ ~~J~~ H	0	1
	E	~~I~~ H	M	1	0
╳	F	~~J~~ H	~~N~~ M	1	0
╳	G	~~K~~ ~~J~~ H	~~P~~ M	1	0
→	H	A	A	0	1
→	I	A	A	0	1
	J	A	–	0	–
→	K	A	–	0	–
t_3 →	L	A	–	0	–
	M	A	–	1	–
╳	N	A	–	1	–
╳	P	A	–	1	–



P.S.	N.S.		Z	
	$x=0$	$x=1$	$x=0$	$x=1$
A	B	C	1	0
B	D	E	1	0
C	E	E	0	1
D	H	H	0	1
E	H	M	1	0
H	A	A	0	1
M	A	–	1	–

State Assignment

$R_1 : (B,C)\,(D,E)\,(H,M)$

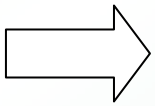
$R_2 : (B,C)\,(D,E)\,(H,M)$

$R_3 : (A,B,E,M)\,(C,D,H)$

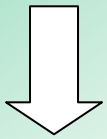
P.S.	x = 0	x = 1	x = 0	x = 1
A	B	C	1	0
B	D	E	1	0
C	E	E	0	1
D	H	H	0	1
E	H	M	1	0
H	A	A	0	1
M	A	–	1	–

Q_1Q_2 \ Q_3	0	1
00	A	
01	B	C
11	M	H
10	E	D

Assignment Map



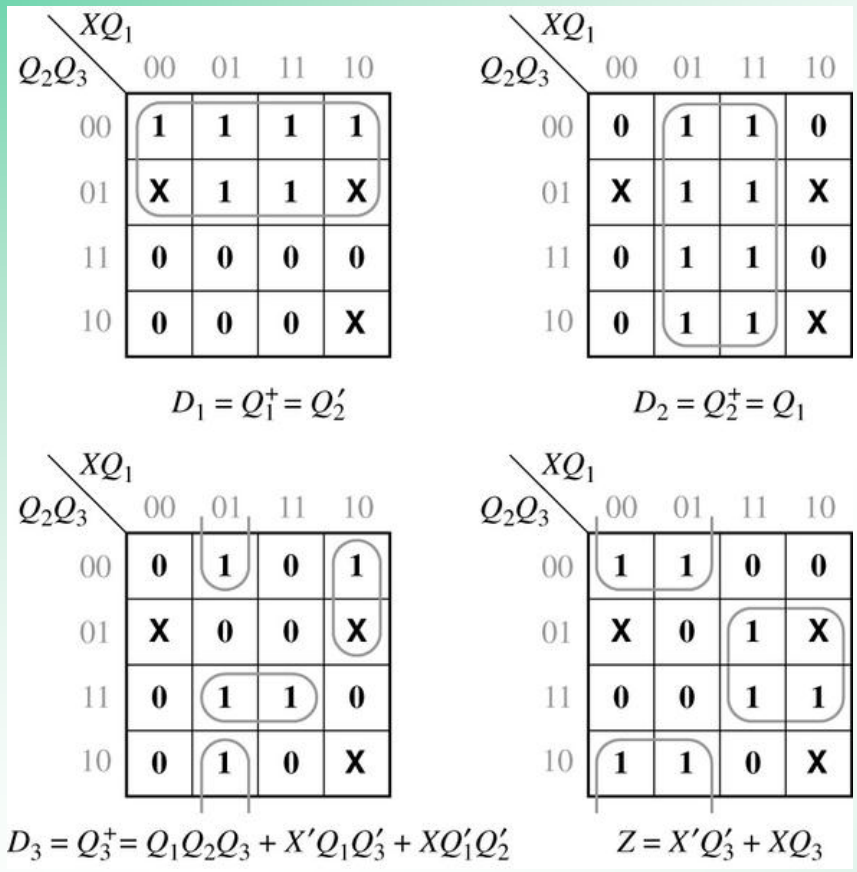
$Q_1\,Q_2\,Q_3$		$Q_1^+\,Q_2^+\,Q_3^+$			
P.S.		N.S.		Z	
		x = 0	x = 1	x = 0	x = 1
A	000	010	011	1	0
B	010	101	100	1	0
C	011	100	100	0	1
D	101	111	111	0	1
E	100	111	110	1	0
H	111	000	000	0	1
M	110	000	– – –	1	–



P.S.	N.S.		Z	
	$x=0$	$x=1$	$x=0$	$x=1$
000	010	011	1	0
001	×××	×××	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	×××	1	×
111	000	000	0	1

Use D F/F

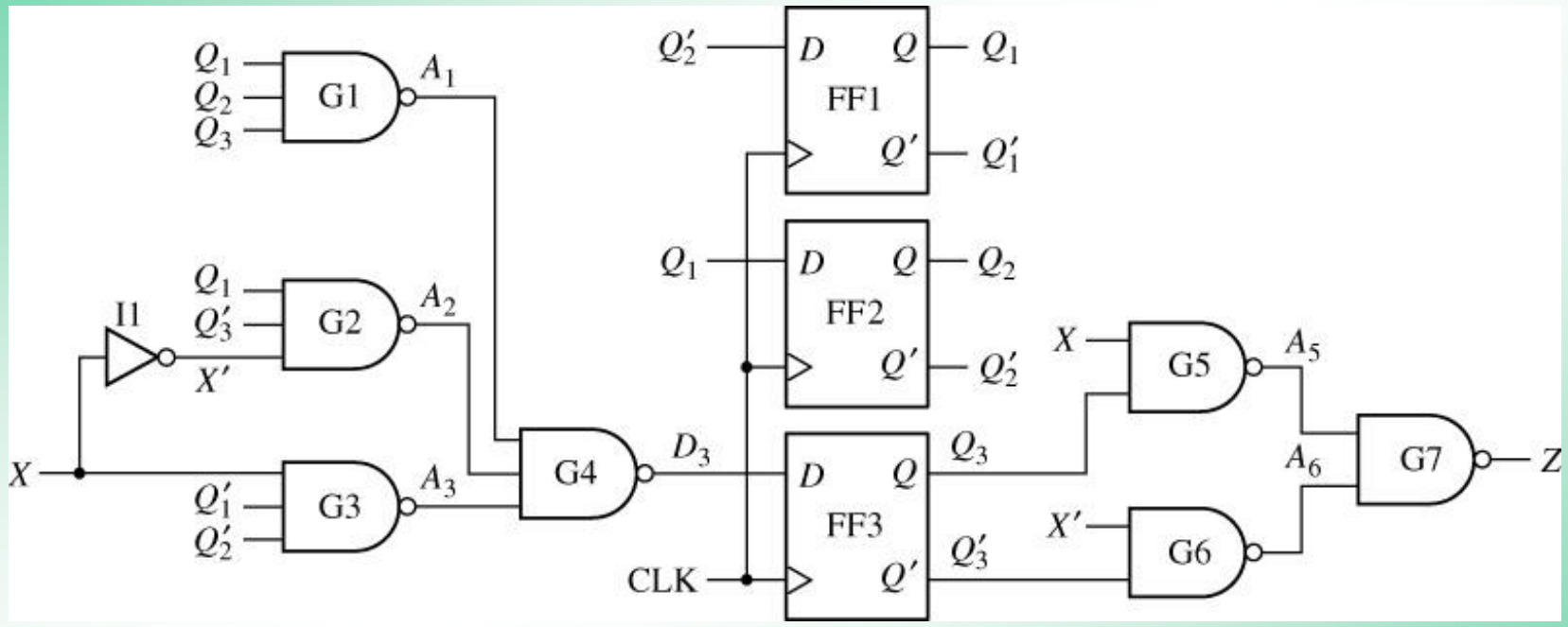
Next - State Maps



P.S.	N.S.		Z	
	x = 0	x = 1	x = 0	x = 1
000	010	011	1	0
001	× × ×	× × ×	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	× × ×	1	×
111	000	000	0	1

Use D F/F

Circuit Diagram



Use J - K F/F

Next - State Maps

Q_1Q_2 \ XQ_3	00	01	11	10
Q_1=0 00	0	X	X	0
J_1 01	1	1	1	1
Q_1=1 11	0	0	0	X
K'_2 10	1	1	1	1

$$J_1 = Q_2$$

$$K_1 = Q_2$$

Q_1Q_2 \ XQ_3	X=0: 00	X=0: 01	X=1: 11	X=1: 10
00	0	1	1	0
01	2	3	3	2
11	6	7	7	6
10	4	5	5	4

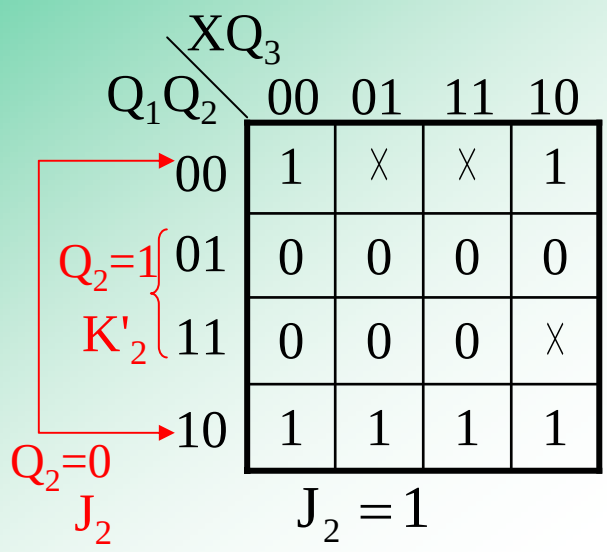
P.S.	N.S.		Z	
	x = 0	x = 1	x = 0	x = 1
000	010	011	1	0
001	× × ×	× × ×	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	× × ×	1	×
111	000	000	0	1

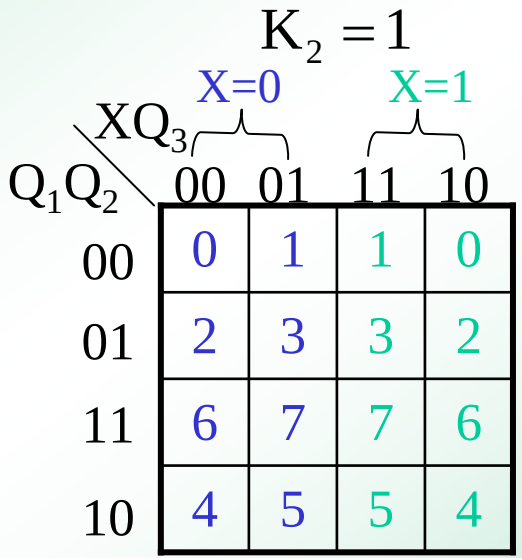
Derivation of Flip-Flop Input Equations from Next State Maps

Type of F/F	Input	Q=0		Q=1		Rules for forming input map from next state map	
		Q+ =0	Q+=1	Q+ = 0	Q+ = 1	Q=0 Half of Map	Q=1 Half of Map
J-K F/F	J	0	1	x	x	No change	Fill in with x's
	K	x	x	1	0	Fill in with x's	Complement

Use J - K F/F

Next - State Maps

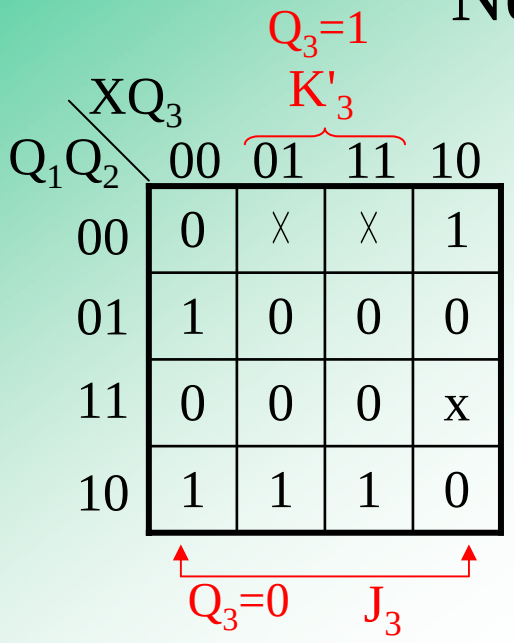




P.S.	N.S.		Z	
	x = 0	x = 1	x = 0	x = 1
000	010	011	1	0
001	× × ×	× × ×	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	× × ×	1	×
111	000	000	0	1

Use J - K F/F

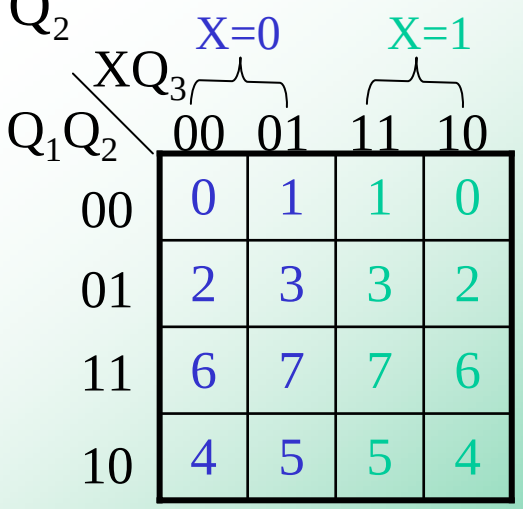
Next - State Maps



P.S.	N.S.		Z	
	x = 0	x = 1	x = 0	x = 1
000	010	011	1	0
001	× × ×	× × ×	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	× × ×	1	×
111	000	000	0	1

$$J_3 = XQ_1'Q_2' + X'Q_1'Q_2 + X'Q_1Q_2'$$

$$K_3 = Q_2$$



Use J - K F/F

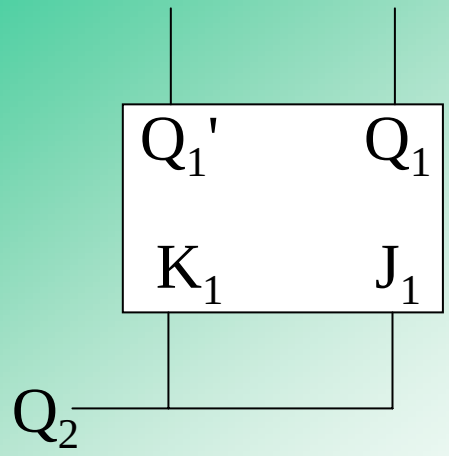
P.S.	N.S.		Z	
	x = 0	x = 1	x = 0	x = 1
000	010	011	1	0
001	× × ×	× × ×	×	×
010	101	100	1	0
011	100	100	0	1
100	111	110	1	0
101	111	111	0	1
110	000	× × ×	1	×
111	000	000	0	1

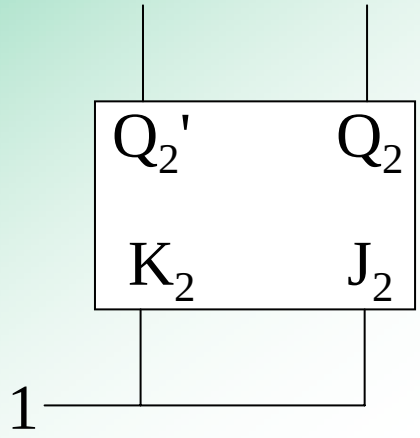
Q_1Q_2 \ XQ_3	00	01	11	10
00	1	X	X	0
01	1	0	1	0
11	1	0	1	X
10	1	0	1	0

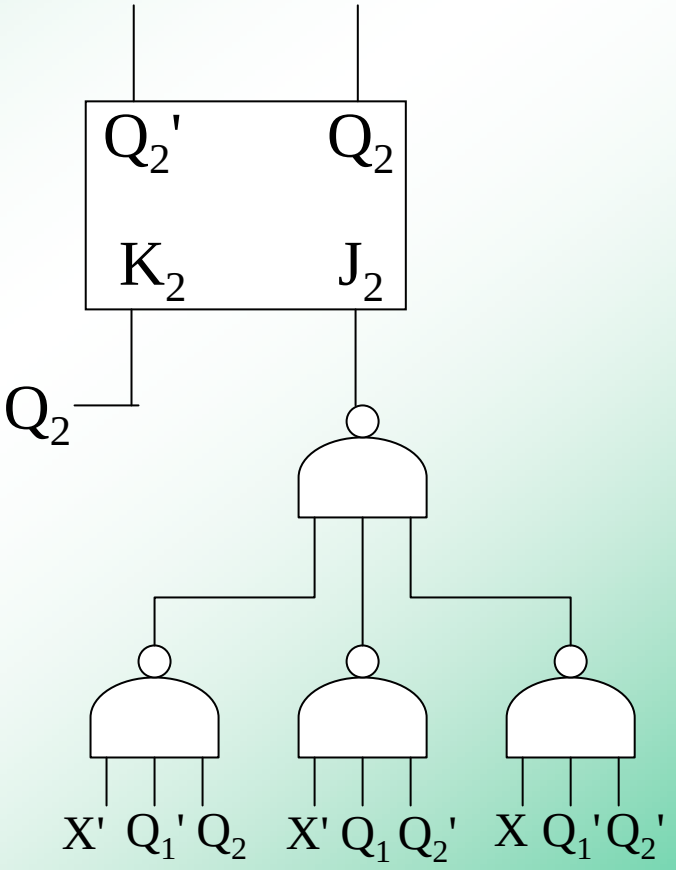
$$Z = X'Q_3' + XQ_3$$

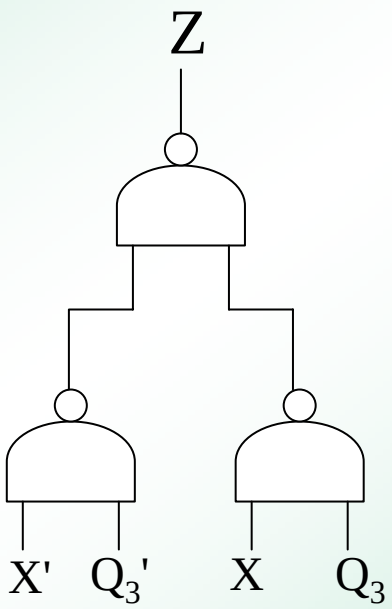
$$= \left[(X'Q_3')'(XQ_3)'\right]'$$

Q_1Q_2 \ XQ_3	00	01	11	10
	X=0		X=1	
00	0	1	1	0
01	2	3	3	2
11	6	7	7	6
10	4	5	5	4


Q_1'
Q_1
K_1
J_1
Q_2

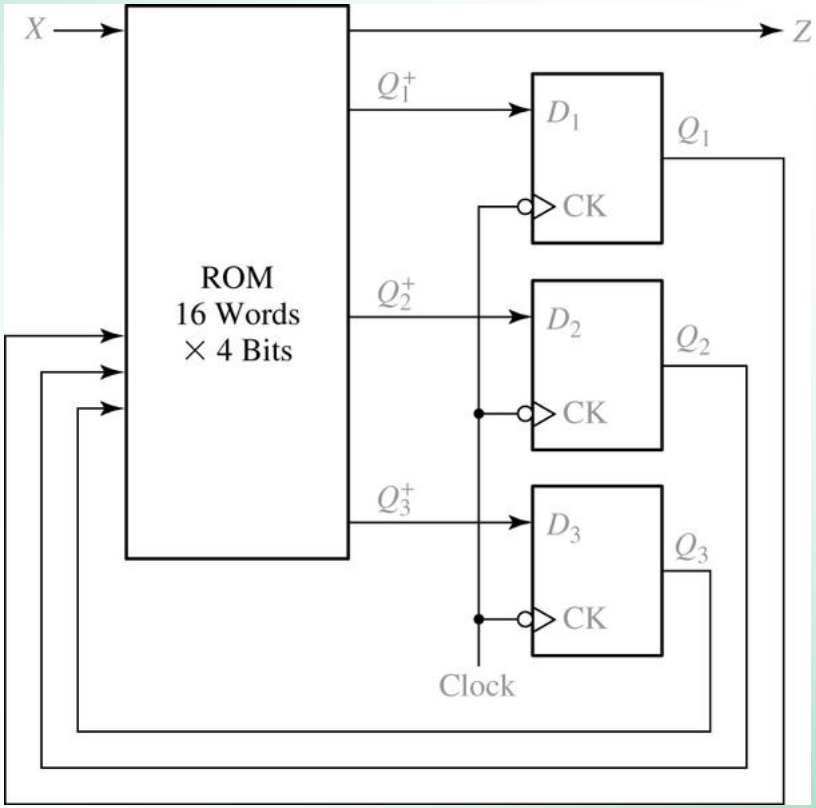

Q_2'
Q_2
K_2
J_2
1


Q_2'
Q_2
K_2
J_2
Q_2
X' Q_1' Q_2
X' Q_1 Q_2'
X Q_1' Q_2'

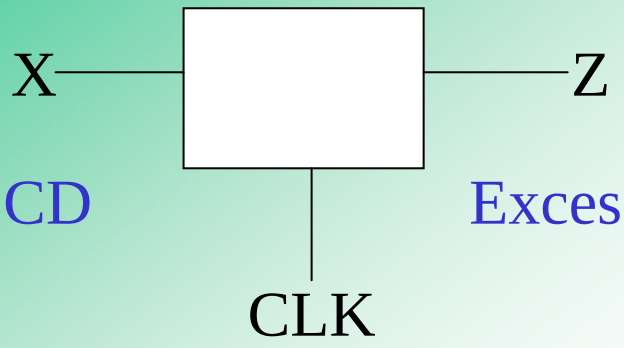

Z
X' Q_3'
X Q_3

16.4 Design of sequential circuits using ROMs and PLAs

ROMs implementation



State Assignment for ROMs



BCD Excess-3 Code

Just binary order is good enough

	x = 0	x = 1	x = 0	x = 1
A	B	C	1	0
B	D	E	1	0
C	E	E	0	1
D	H	H	0	1
E	H	M	1	0
H	A	A	0	1
M	A	–	1	–

	$Q_1 Q_2 Q_3$	$Q_1^+ Q_2^+ Q_3^+$		Z	
	P.S.	N.S.			
		x = 0	x = 1	x = 0	x = 1
A	000	001	010	1	0
B	001	011	100	1	0
C	010	100	100	0	1
D	011	101	101	0	1
E	100	101	110	1	0
H	101	000	000	0	1
M	110	000	– – –	1	–

ROMs implementation

	$Q_1 Q_2 Q_3$ P.S.	$Q_1^+ Q_2^+ Q_3^+$ N.S.		Z	
		$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	000	001	010	1	0
B	001	011	100	1	0
C	010	100	100	0	1
D	011	101	101	0	1
E	100	101	110	1	0
H	101	000	000	0	1
M	110	000	– – –	1	–

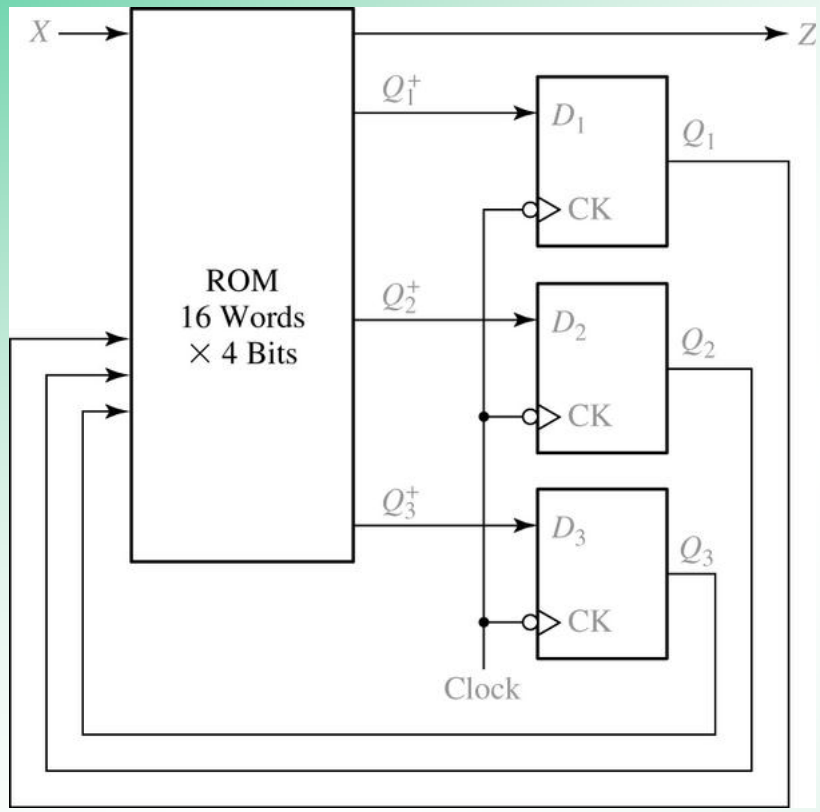
$$Z = \sum m(0,1,4,6,10,11,13) + \sum d(7,14,15)$$

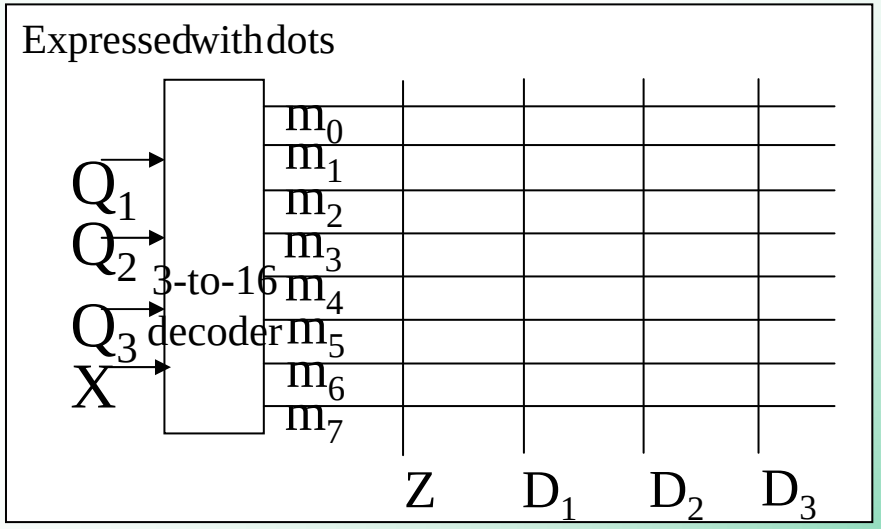
$$D_1 = \sum m(2,3,4,9,10,11,12) + \sum d(7,14,15)$$

$$D_2 = \sum m(1,8,12) + \sum d(7,14,15)$$

$$D_3 = \sum m(0,1,3,4,11) + \sum d(7,14,15)$$

ROMs implementation



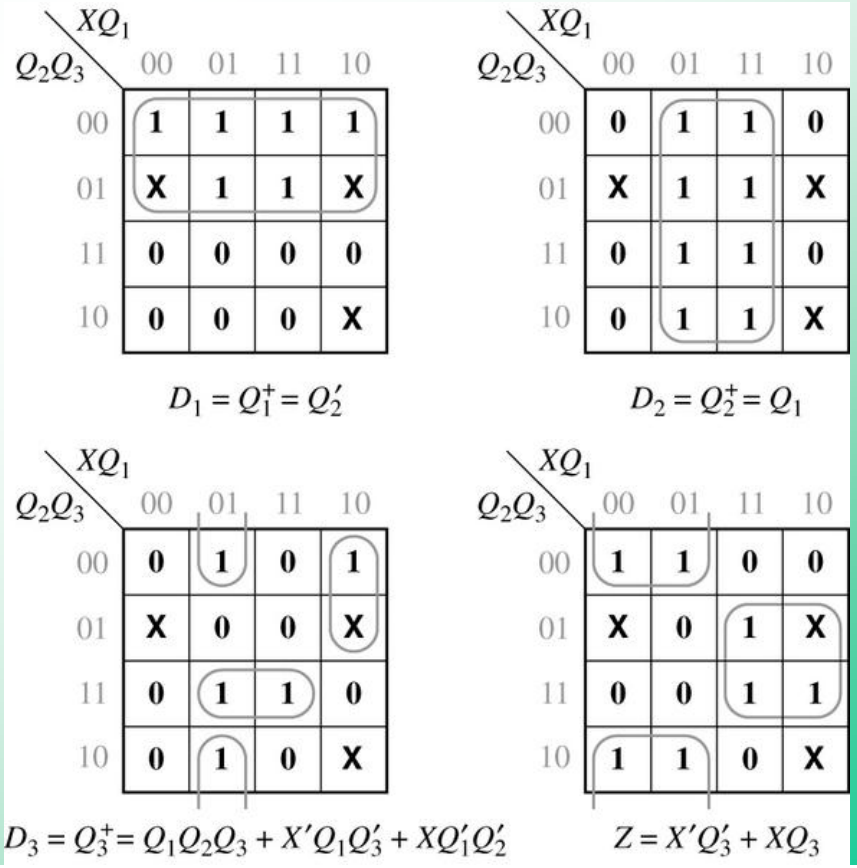


PLA implementation

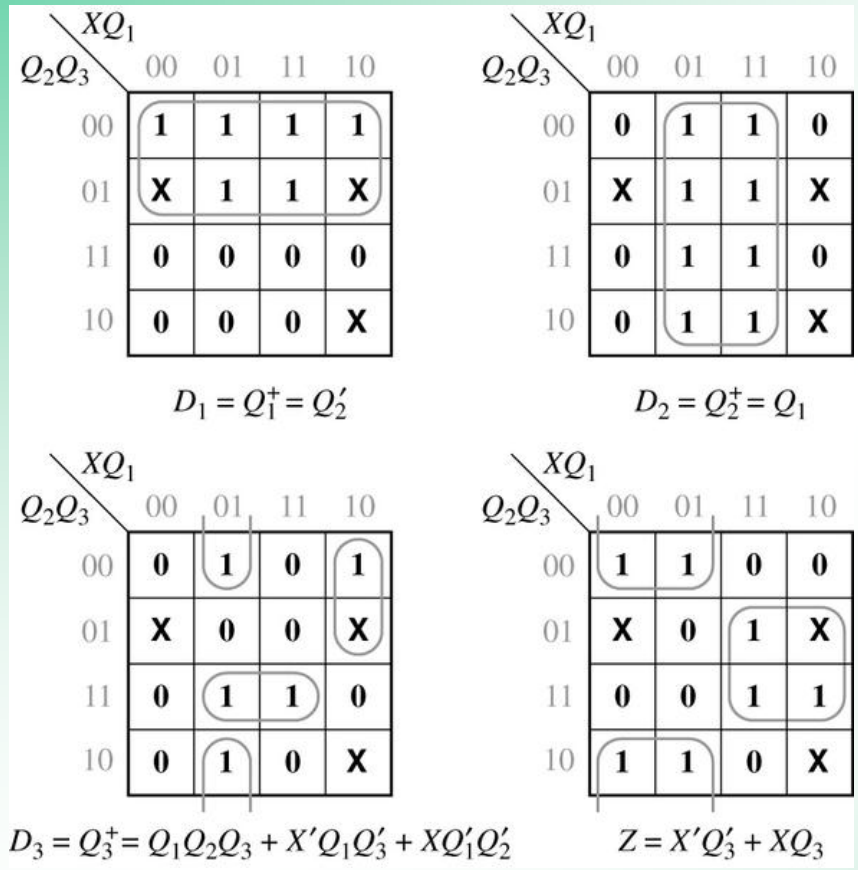
State Assignment is important. Use the adjacent state guideline.

Case1. Direct straight binary order assignment
-> four input, 13 product terms, and four outputs
=> Little reduction

Case2. Use the adjacent state guideline

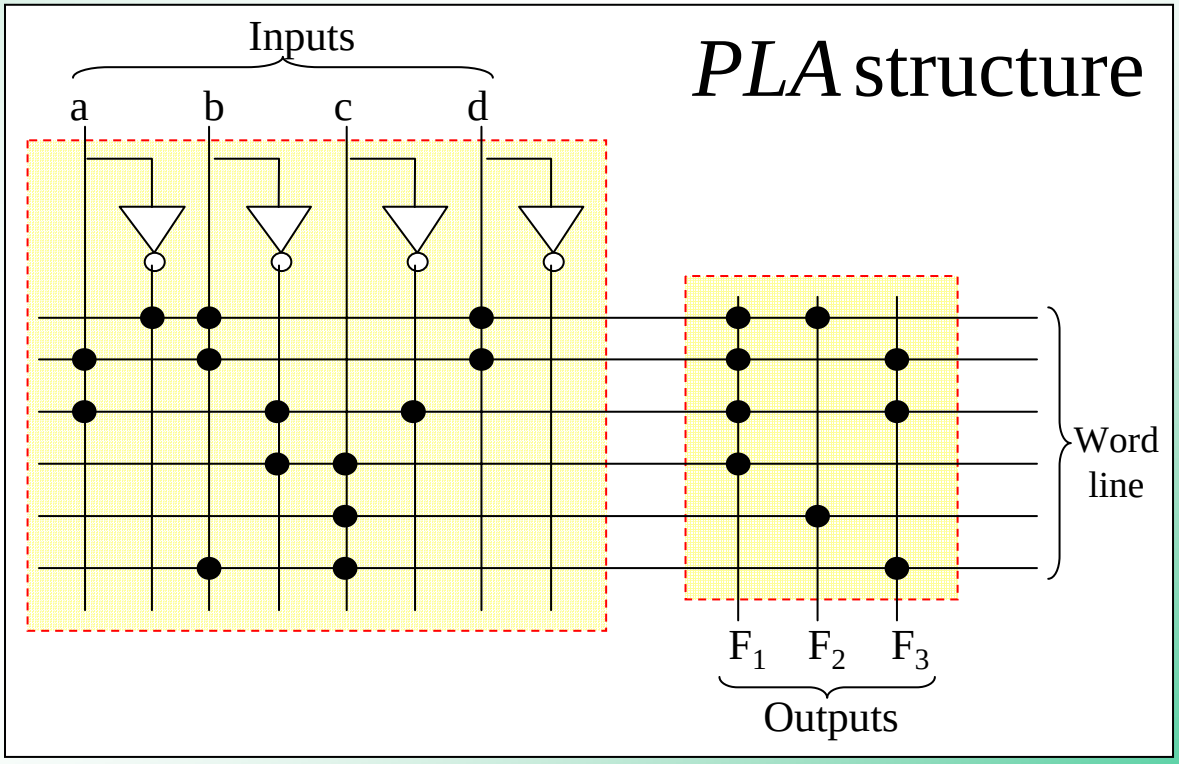


PLA Table

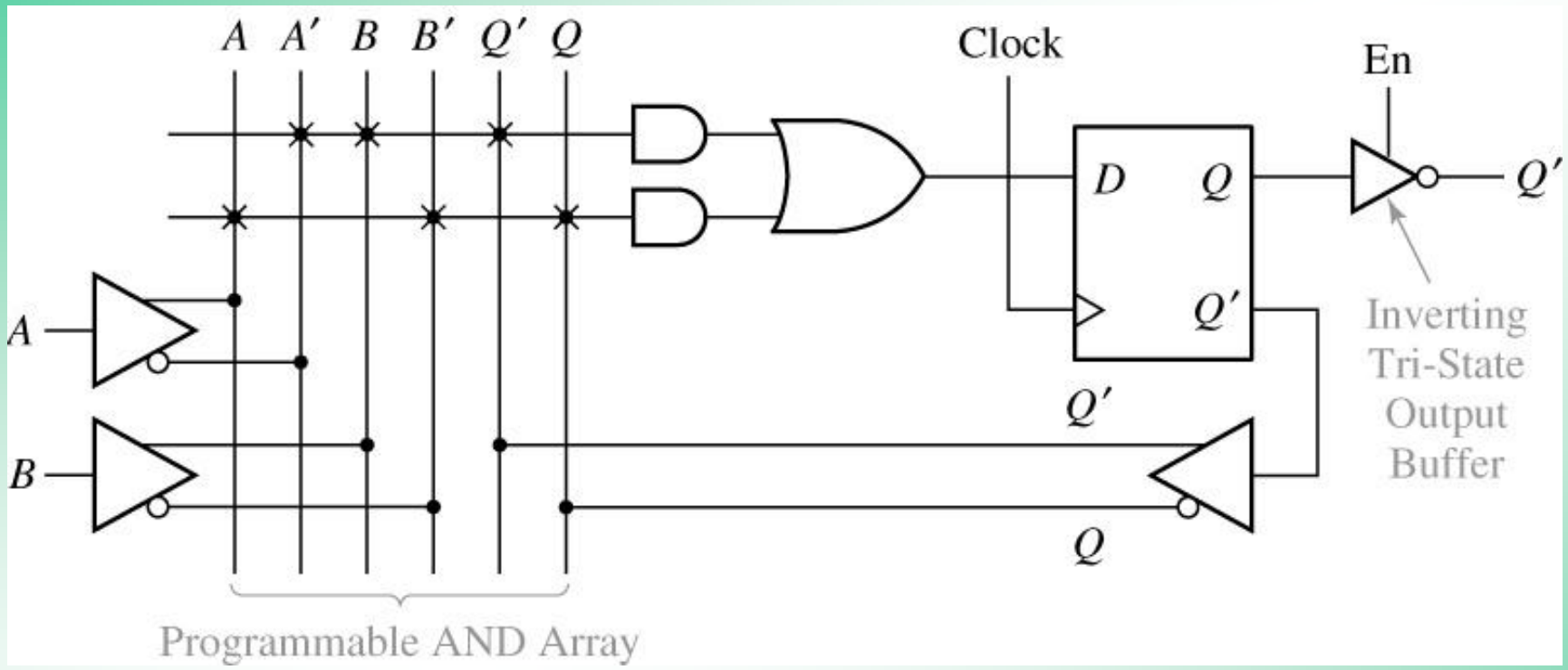


X Q_1 Q_2 Q_3	Z D_1 D_2 D_3
--0-	0100
-1--	0010
-111	0001
01-0	0001
100-	0001
0--0	1000
1--1	1000

a	b	c	d	F_1	F_2	F_3
0	1	–	1	1	1	0
1	1	–	1	1	0	1
1	0	0	–	1	0	1
–	0	1	–	1	0	0
–	–	1	–	0	1	0
–	1	1	–	0	0	1



PLA implementation



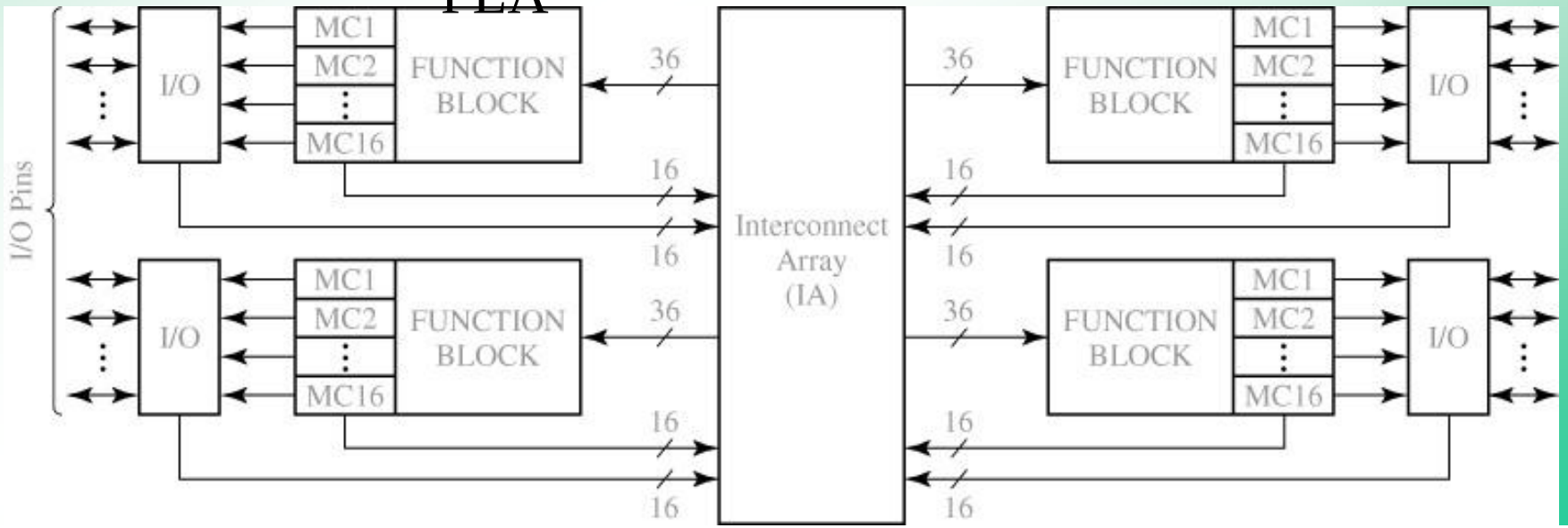
16-5 Sequential Circuit Design Using CPLDs

Integrate and interconnect many PALs and PLAs on a single chip

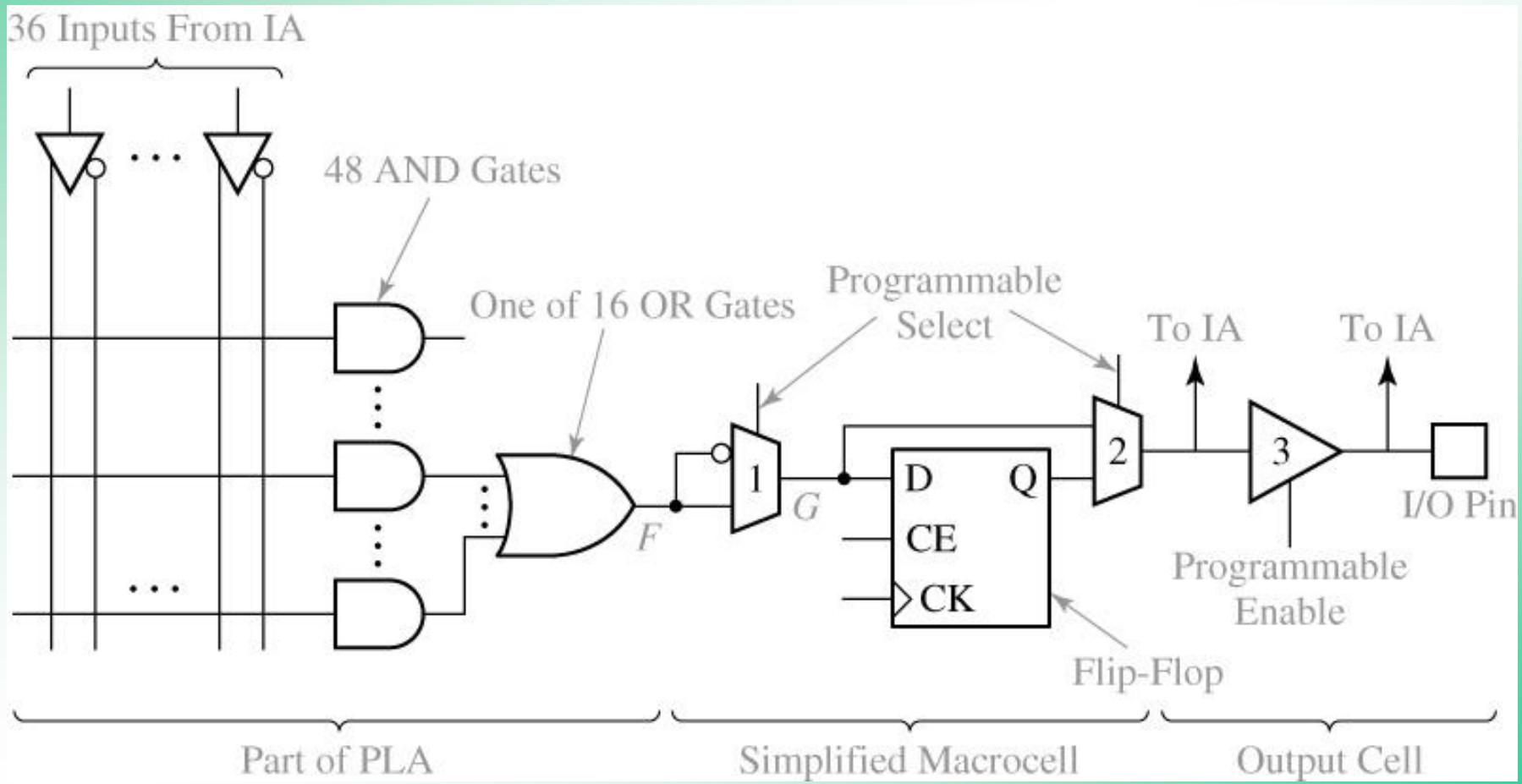
- *PLA to form combinational logic*
- *Macro Cell*
  - *Register for Sequential Logic*
  - *Pass Through for Combinational Logi*
- *I/O Cell*
  - *Three State Buffer for Bidirectional I/C*
  - *Input Latch to synchronize inputs*
- *Floating Gate Programmable*

Xilinx XCR3054XL CPLD

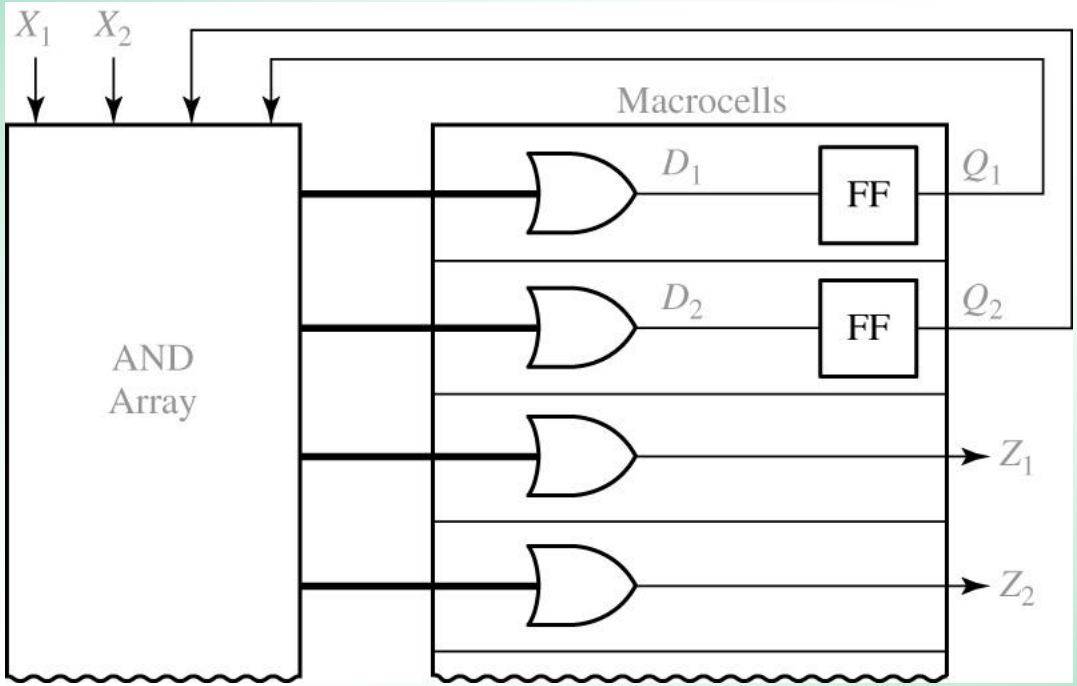
PLA



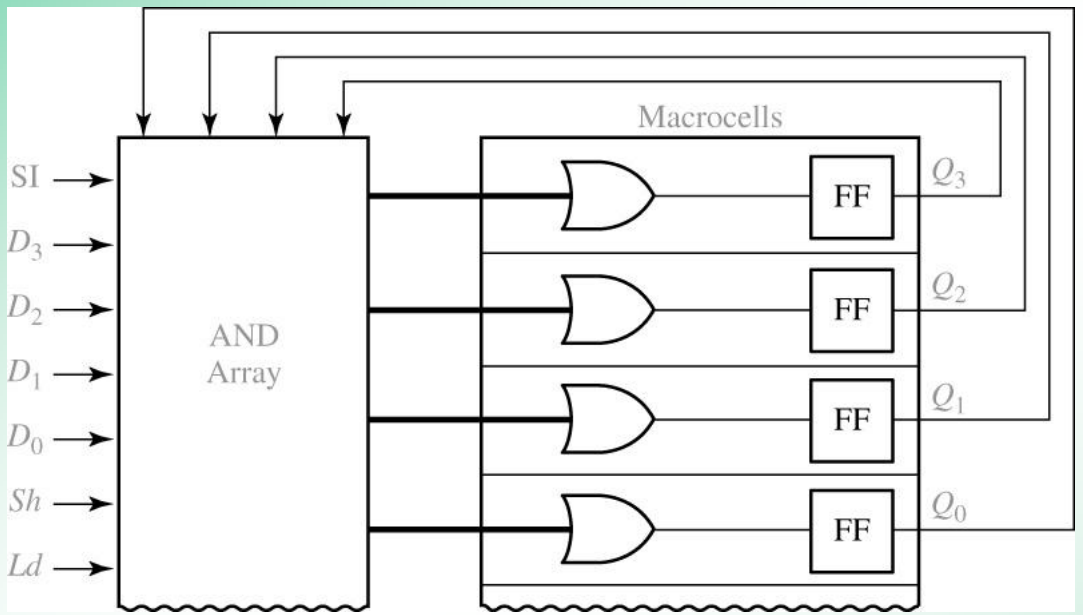
CPLD Function block an macrocell



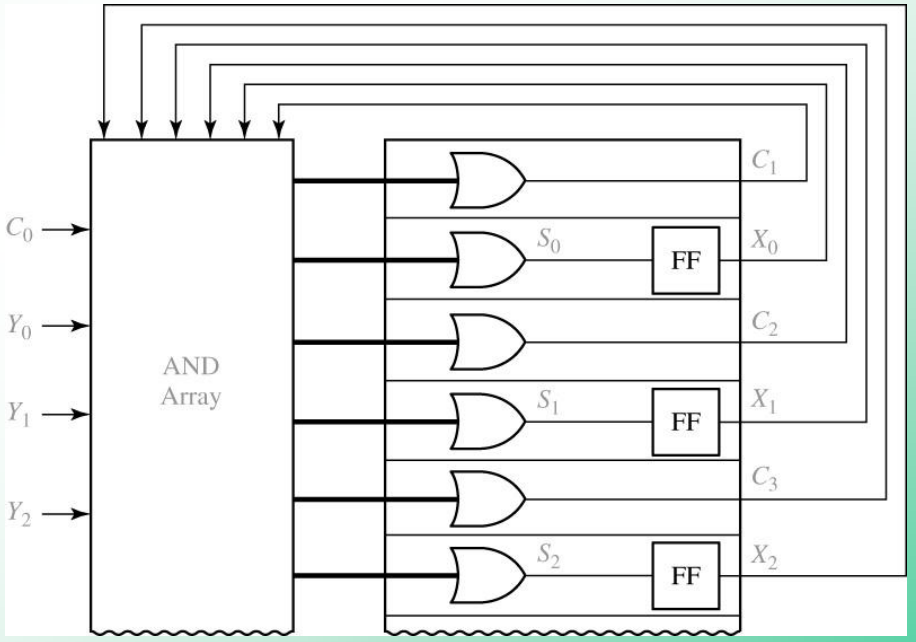
CPLD implementation of a Mealy Machine



Shift registers

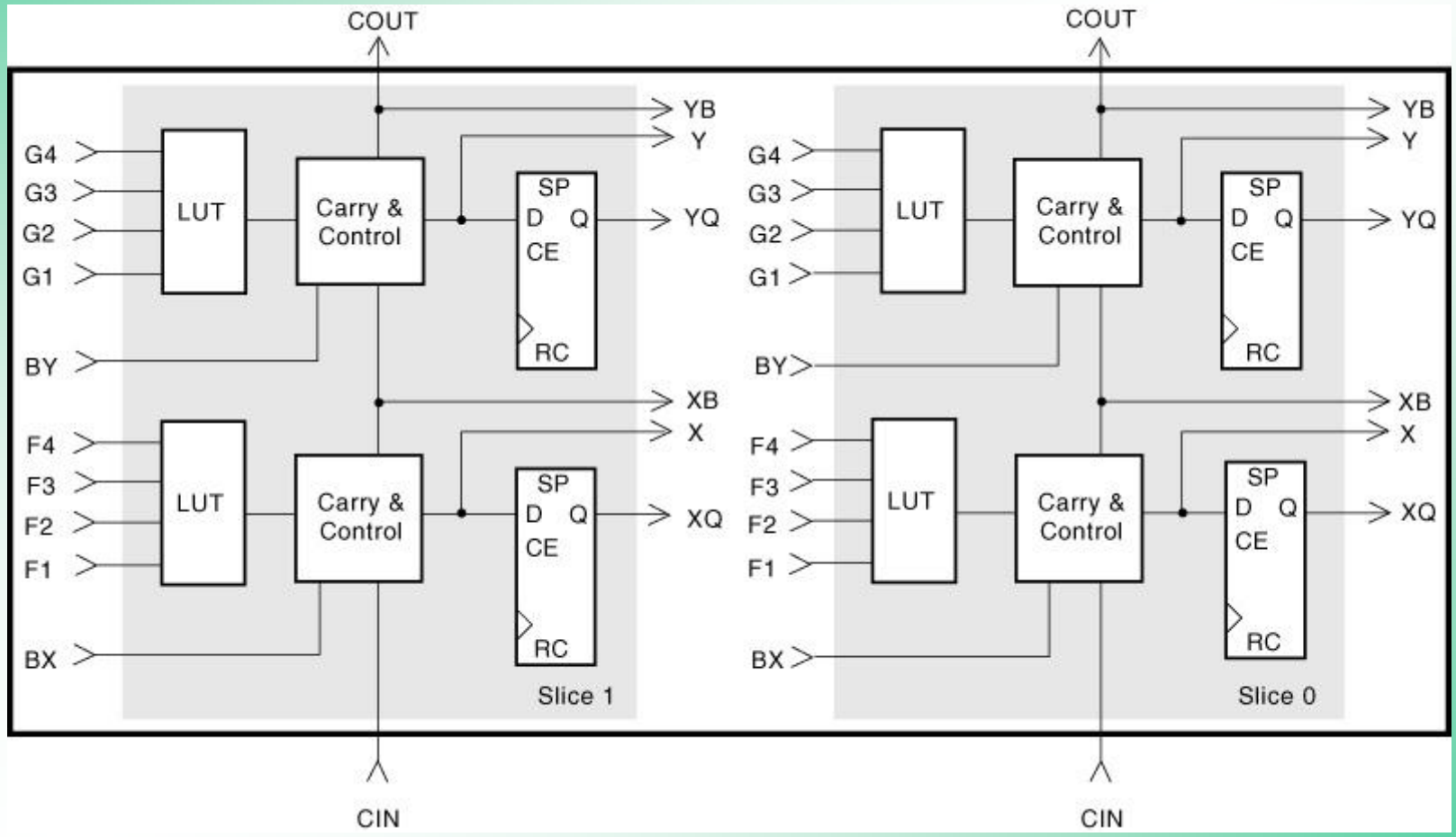


A Parallel adder
with accumulator

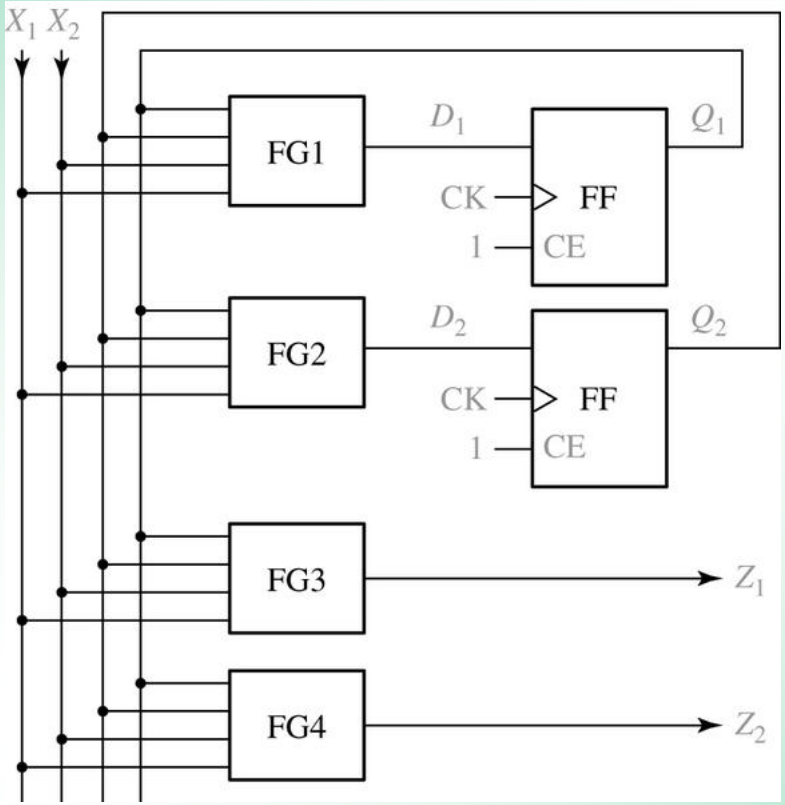


16-6 Sequential Circuit Design Using FPGAs

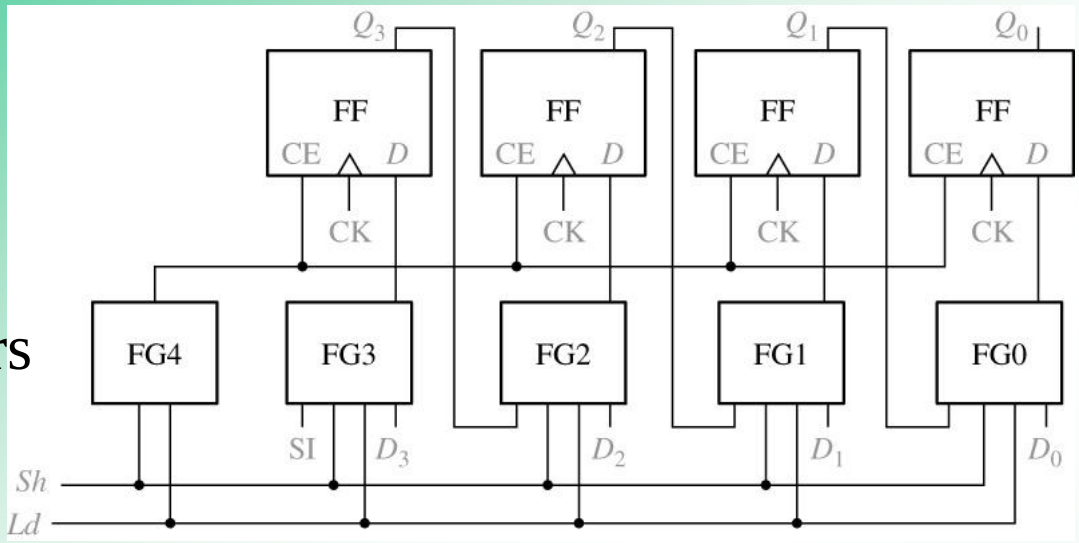
Typical FPGA circuits



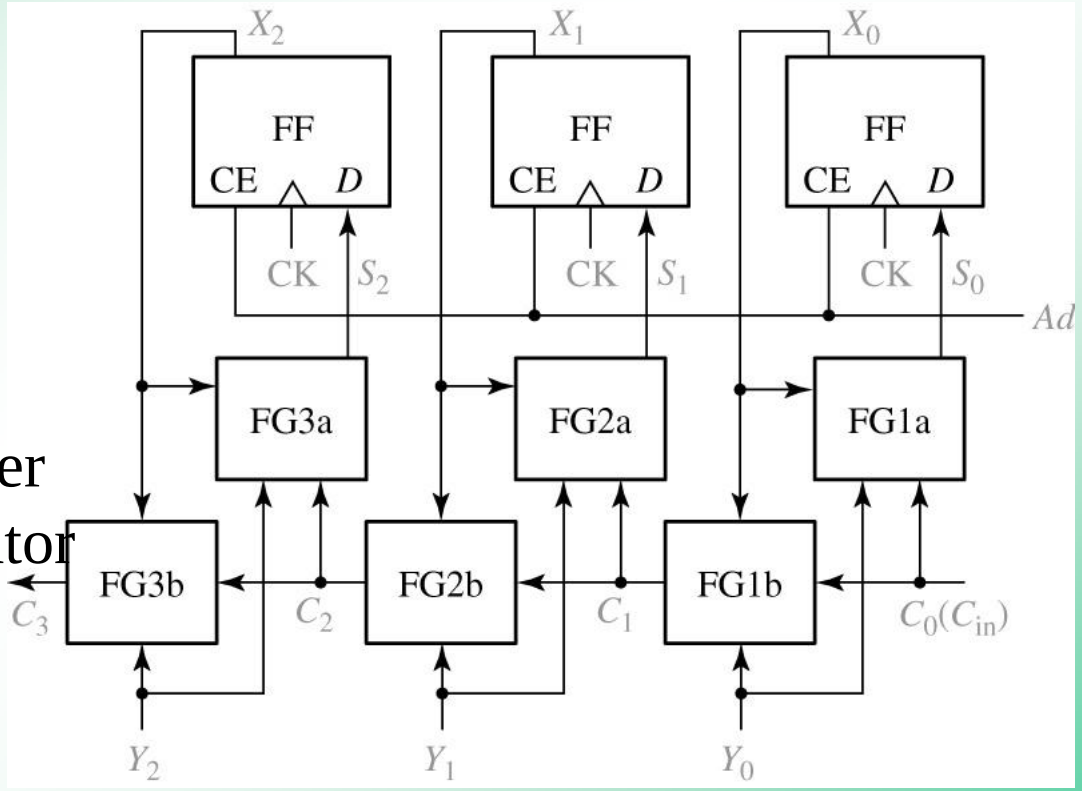
implementation of a Mealy Machine



Shift registers



A Parallel adder with accumulator



HOMEWORK -- Unit 16

- 16.1
- 16.2
- 16.3
- 16.5
- 16.6