Chap 14:

Derivation of State Graph and Table

Sequential Circuit Design

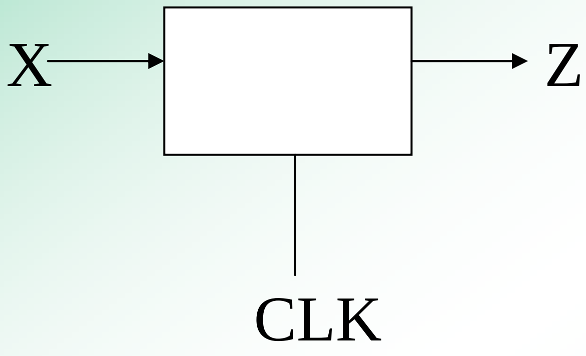
- To design a sequential circuit, given a problem statement,
  - 1. construct a state table or state graph (unit 14)
    - Further simplification (unit 15)
  - 2. derive FF input eq. and output eq. (in unit 12)

14-1 Design of a Sequence Detector

Given problem statement $\Rightarrow$ state graph

state table

– Mealy Machine –

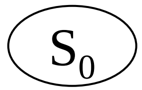


Z gives "1" when X is "101"

X	=	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	0	
Z	=	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	
(Time	:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	)

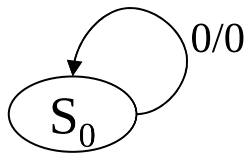
*Construction of state graph

Start with a reset state S_0

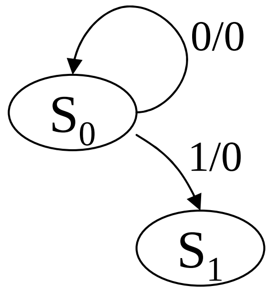


1

S_0 : receives a "0" $\Rightarrow$ stays at S_0 , $Z = 0$



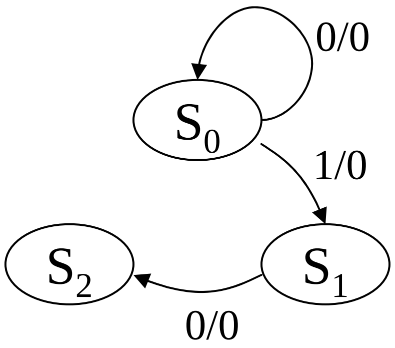
receives a "1" $\Rightarrow$ a new state S_1 , $Z = 0$



2

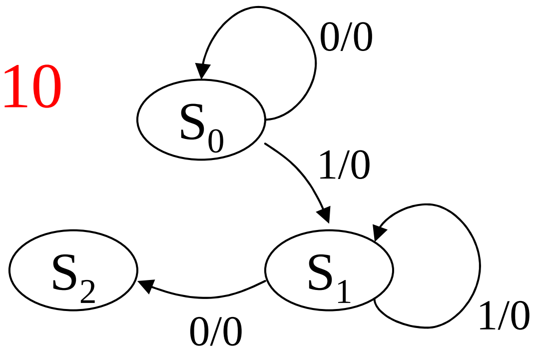
S_1 : receives "0" $\Rightarrow S_2$, $Z = 0$

010



receives "1" $\Rightarrow S_1$, $Z = 0$

0110



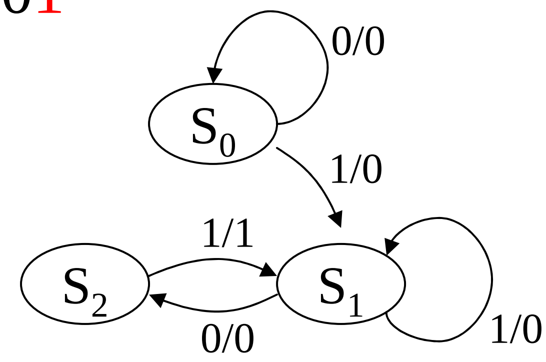
3

Go back to S_1 since it is also the first 1 in new sequence

S_2 : receives "1" $\Rightarrow Z = 1$

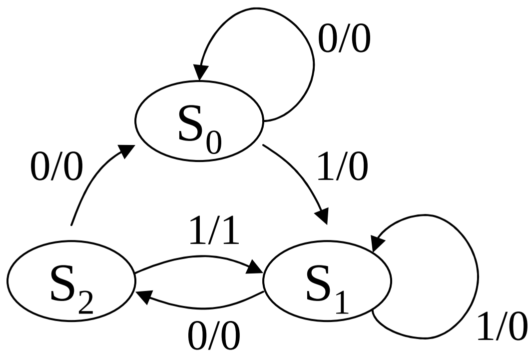
and goes back to S_1

0101



receives "0" $\Rightarrow S_0$, $Z = 0$

0100

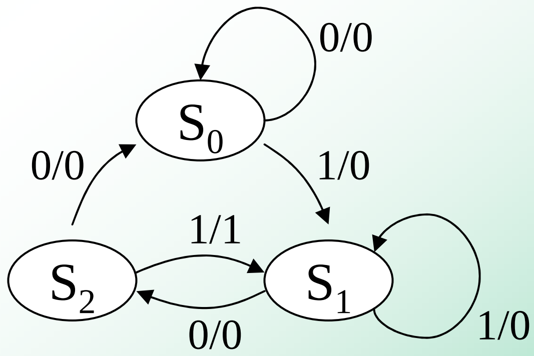


Go back to S_0 since 00 is not a part of desired sequence

4

＊State Table

P.S.	N.S. X = 0	N.S. X = 1	Output Z X = 0	Output Z X = 1
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1



＊State Assignment

A F/F can code 2 states

$\Rightarrow$ 3 states $\rightarrow$ 2 F/Fs (A , B)

S_0 : AB = 00

S_1 : AB = 01

S_2 : AB = 10

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z X = 0	Z X = 1
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

✻ Choose F/F

Ex : use D - F/F

AB	A^+B^+ X = 0		A^+B^+ X = 1		D_A X = 0	D_A X = 1	D_B X = 0	D_B X = 1
00	0	0	0	1	0	0	0	1
01	1	0	0	1	1	0	0	1
10	0	0	0	1	0	0	0	1

✻ K - map Simplification

AB \ X	0	1
00	0	0
01	1	0
11	x	x
10	0	0

$A^+ = X'B$

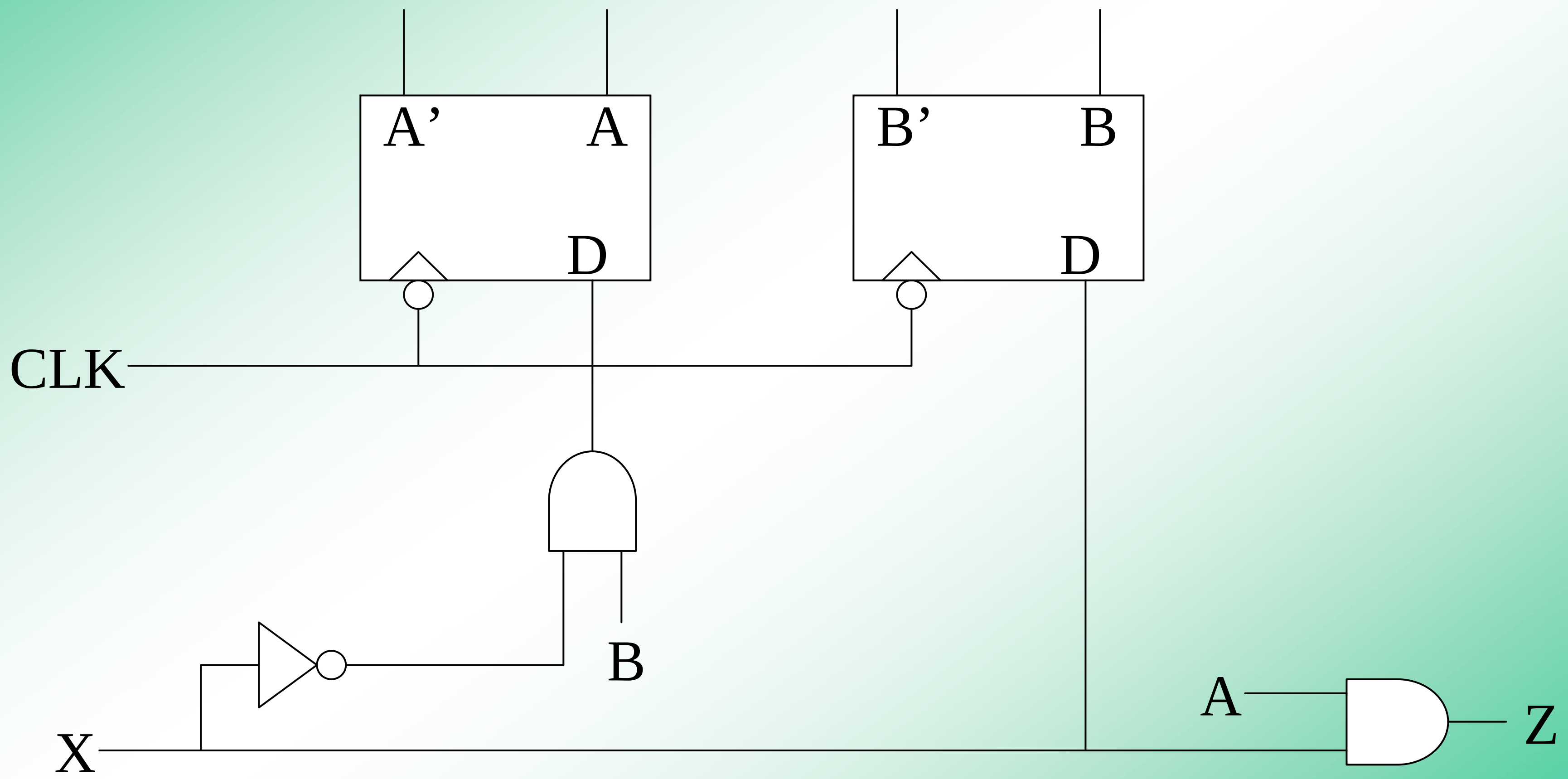
AB \ X	0	1
00	0	1
01	0	1
11	x	x
10	0	1

$B^+ = X$

AB \ X	0	1
00	0	0
01	0	0
11	x	x
10	0	1

$Z = XA$

* Circuit Realization



$$A^+ = D_A = X'B \quad B^+ = D_B = X \quad Z = XA$$

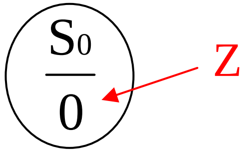
– Moore Machine –

*Construction of state graph

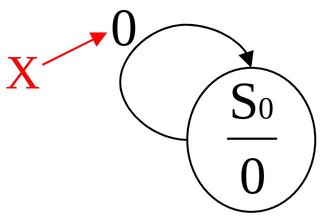
Start with a reset state S_0

$S_0 : Z = 0$

0

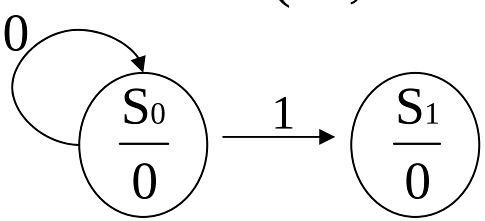


receives "0" $\Rightarrow S_0$



receives "1" $\Rightarrow S_1$ $(S_1, Z = 0)$

01

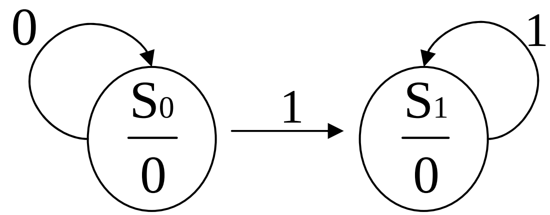


1

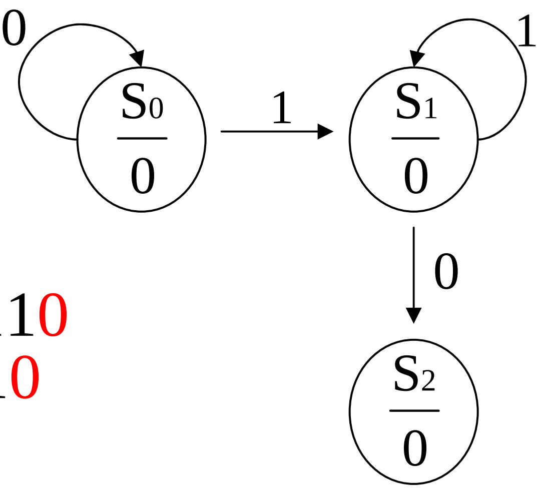
$S_1 : Z = 0$

receives "1" $\Rightarrow S_1$

011



receives "0" $\Rightarrow S_2$ $(Z = 0)$



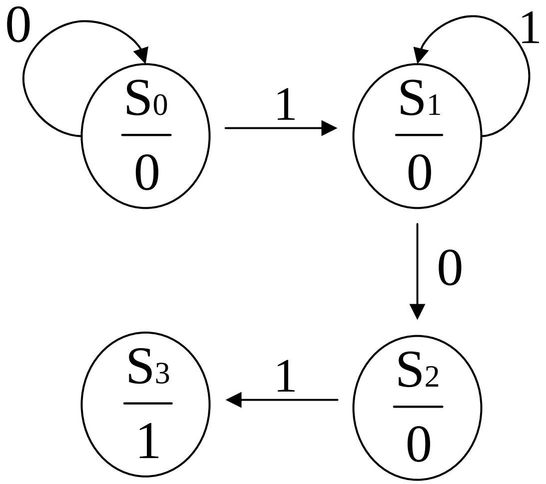
0110

010

2

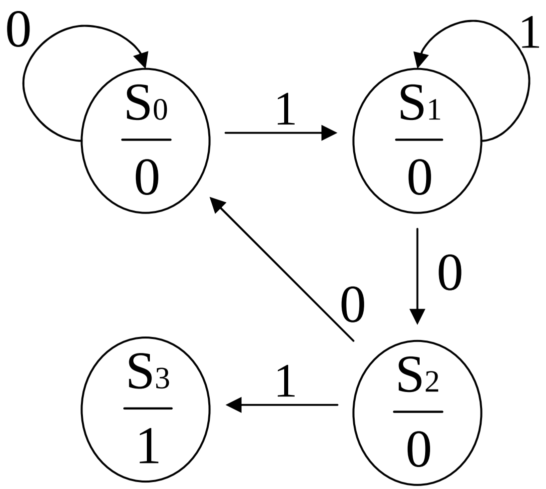
S_2: $Z=0$

receives "1" ⇒ S_3 ($Z=1$)



0101

receives "0" ⇒ S_0

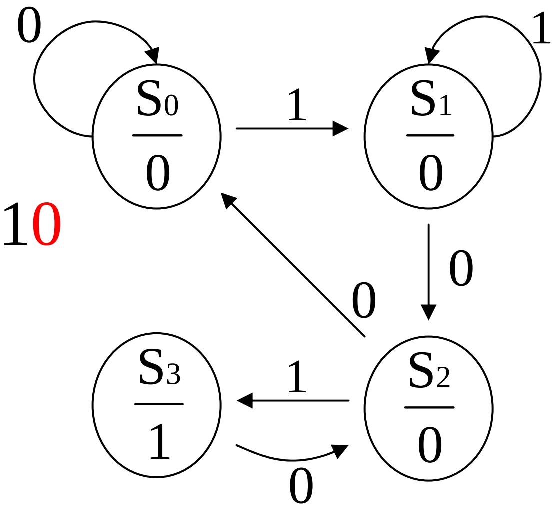


0100

3

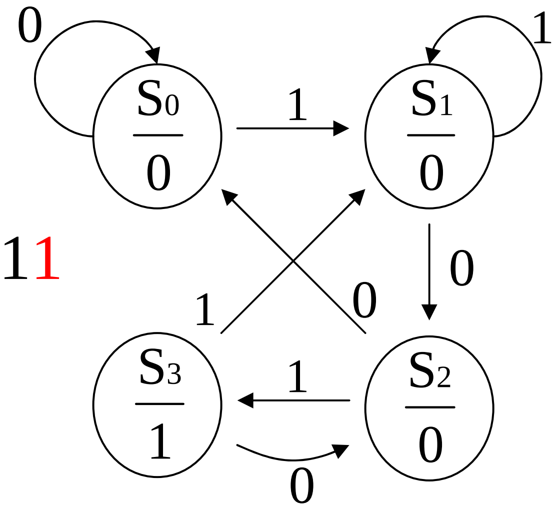
S_3: $Z=1$

receives "0" ⇒ S_2



01010

receives "1" ⇒ S_1

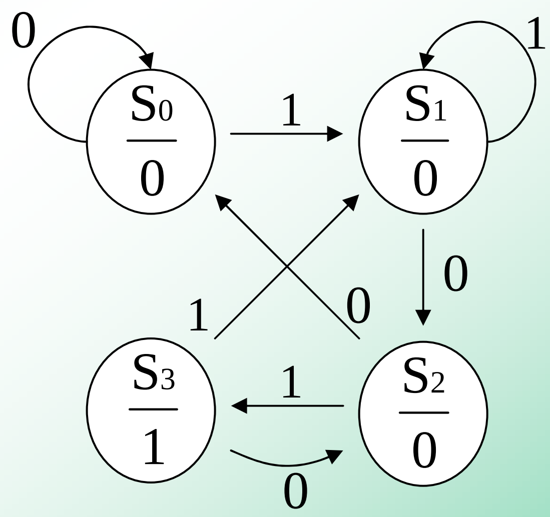


01011

4

✻State Table

P.S.	N.S. X = 0	N.S. X = 1	Present Output Z
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	***1***



✻State Assignment

4 states $\Rightarrow$ 2 F/Fs (A , B)

	AB	A^+B^+ X = 0	A^+B^+ X = 1	Z
S_0	00	00	01	0
S_1	01	11	01	0
S_2	11	00	10	0
S_3	10	11	01	1

✻Choose F/F

use D - F/F

AB	A^+B^+ X = 0	A^+B^+ X = 1	D_A X = 0	D_A X = 1	D_B X = 0	D_B X = 1
00	0 0	0 1	0	0	0	1
01	1 1	0 1	1	0	1	1
11	0 0	1 0	0	1	0	0
10	1 1	0 1	1	0	1	1

✻K - map Simplification

AB \ X	0	1
00	0	0
01	1	0
11	0	1
10	1	0

$A^+ = X'A'B + XAB$

$+ X'AB'$

AB \ X	0	1
00	0	1
01	1	1
11	0	0
10	1	1

$B^+ = XA' + A'B$

$+ AB'$

B \ A	0	1
0	0	1
1	0	0

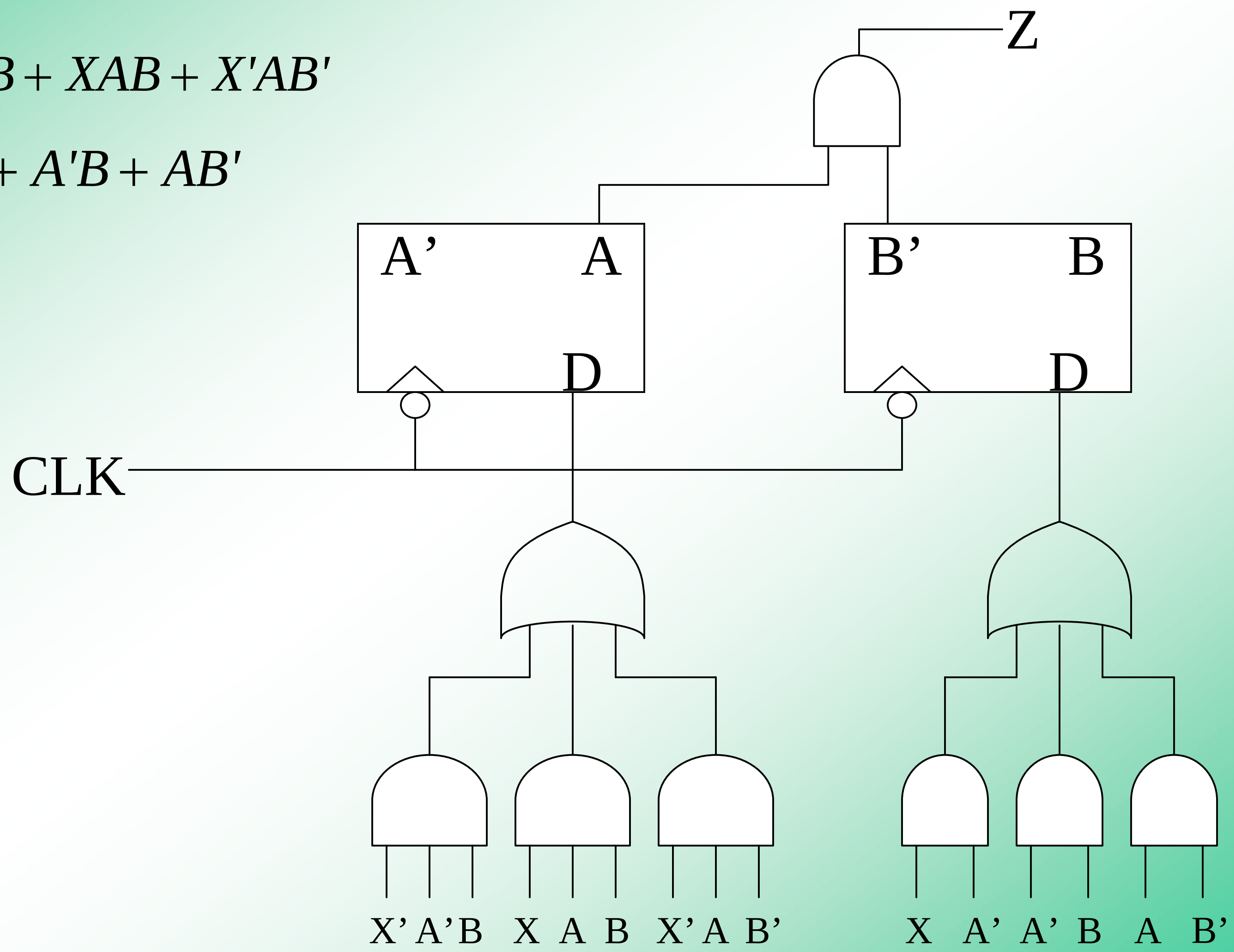
$Z = AB'$

* Circuit Realization

$$A^{+} = X'A'B + XAB + X'AB'$$

$$B^{+} = XA' + A'B + AB'$$

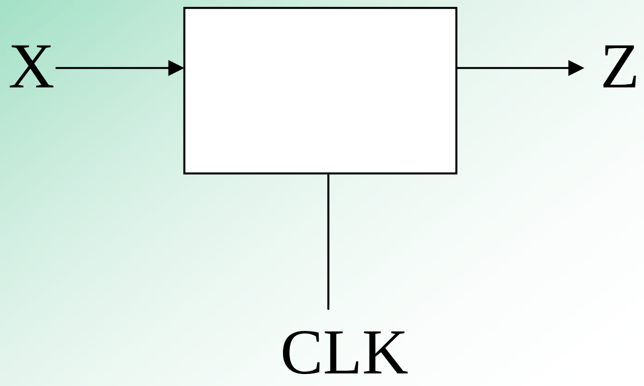
$$Z = AB'$$



14-2 More Complex Problems

– Mealy Machine Example –

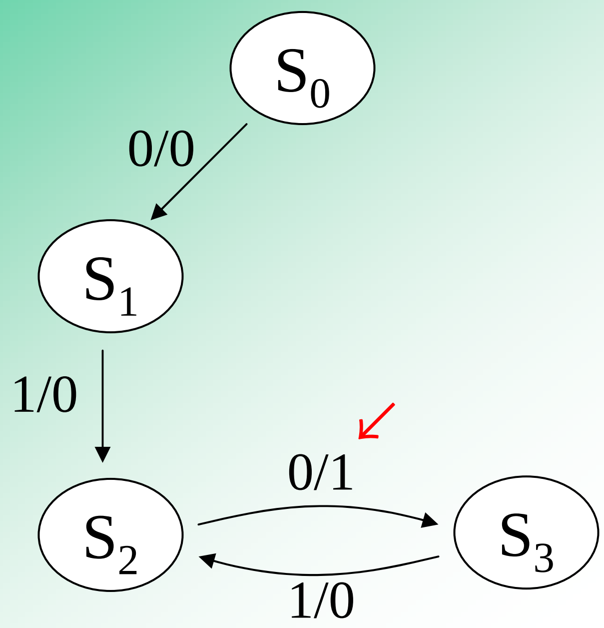
Sequence dectector



Z gives "1" if X = 010 or 1001

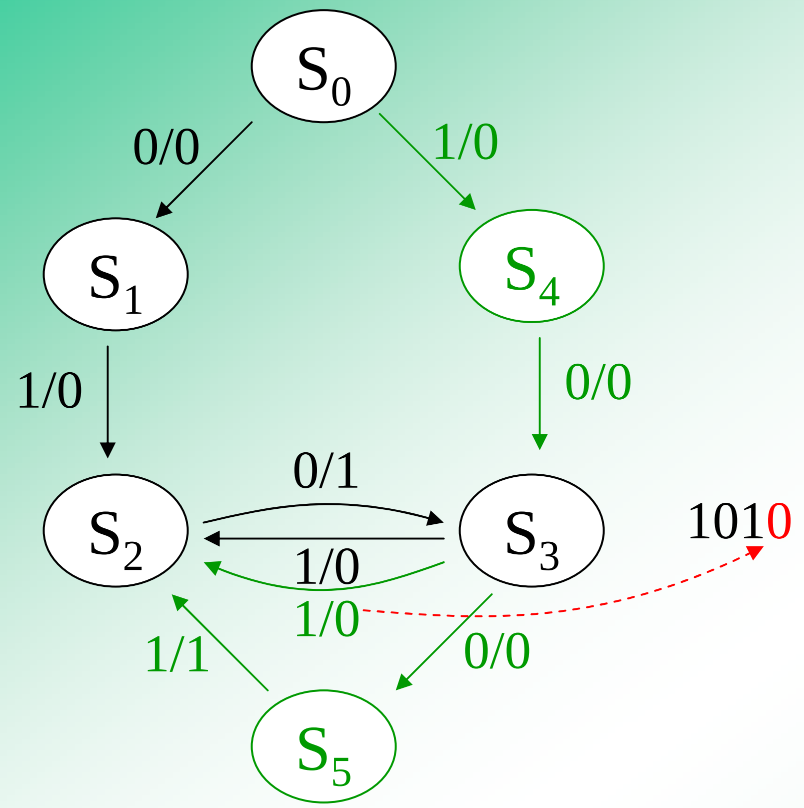
Otherwise, Z = 0

X	=	0	0	1	0	1	0	0	1	0	0	0	1	0	0	1	1	0
Z	=	0	0	0	1	0	1	0	1	1	0	0	0	1	0	1	0	0



State	Sequence received
S_0	reset
S_1	0
S_2	01
S_3	010

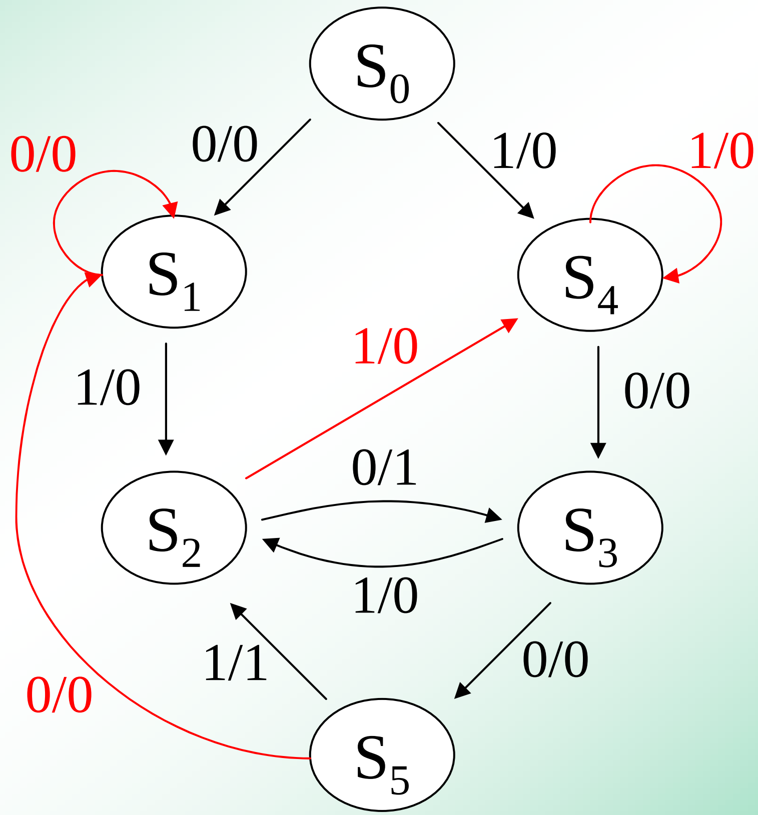
partial state graph construction for 010



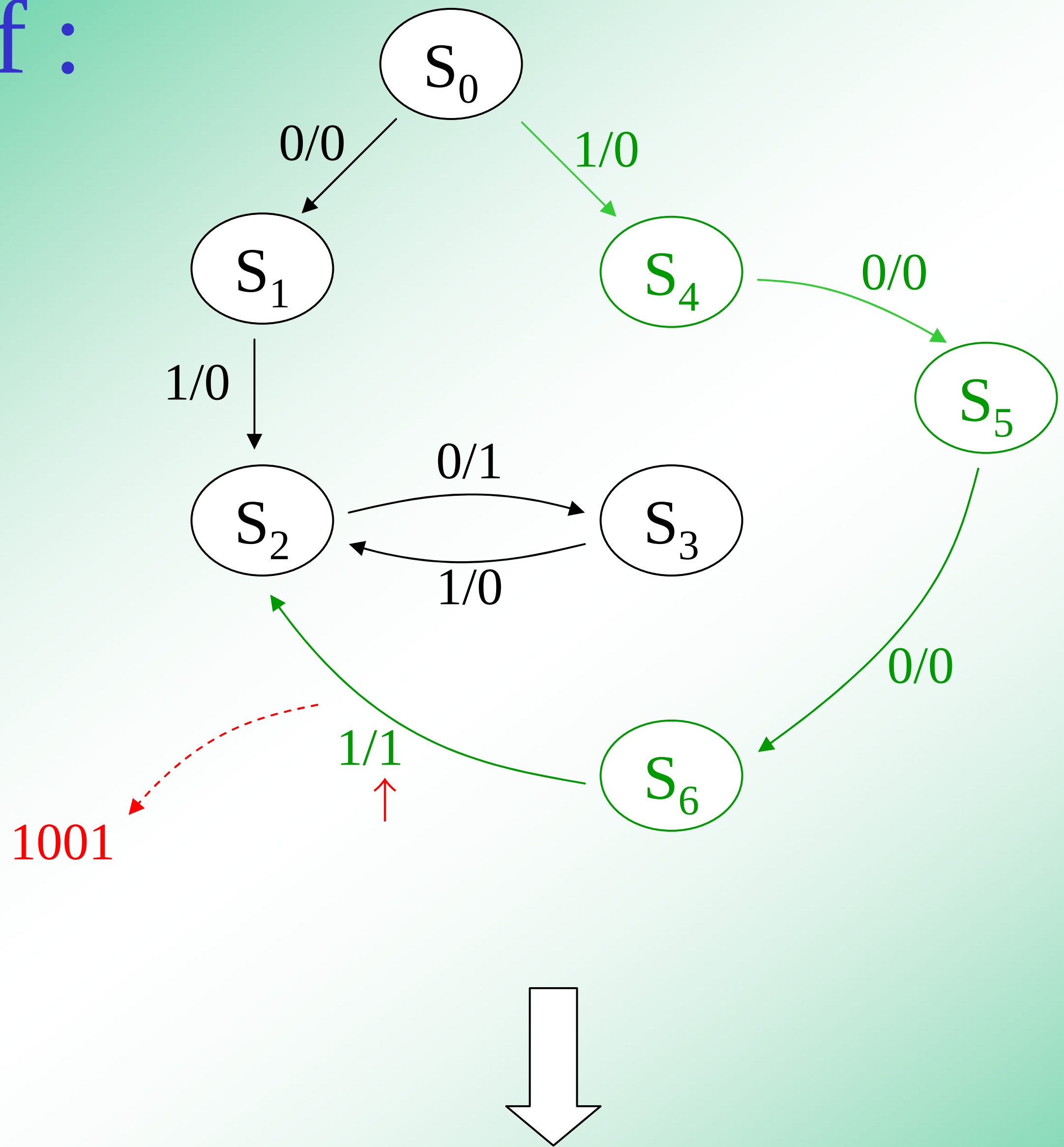
State	Sequence received
S_0	reset
S_1	0
S_2	01
S_3	010 or 10
S_4	1
S_5	100

partial state graph construction for 1001

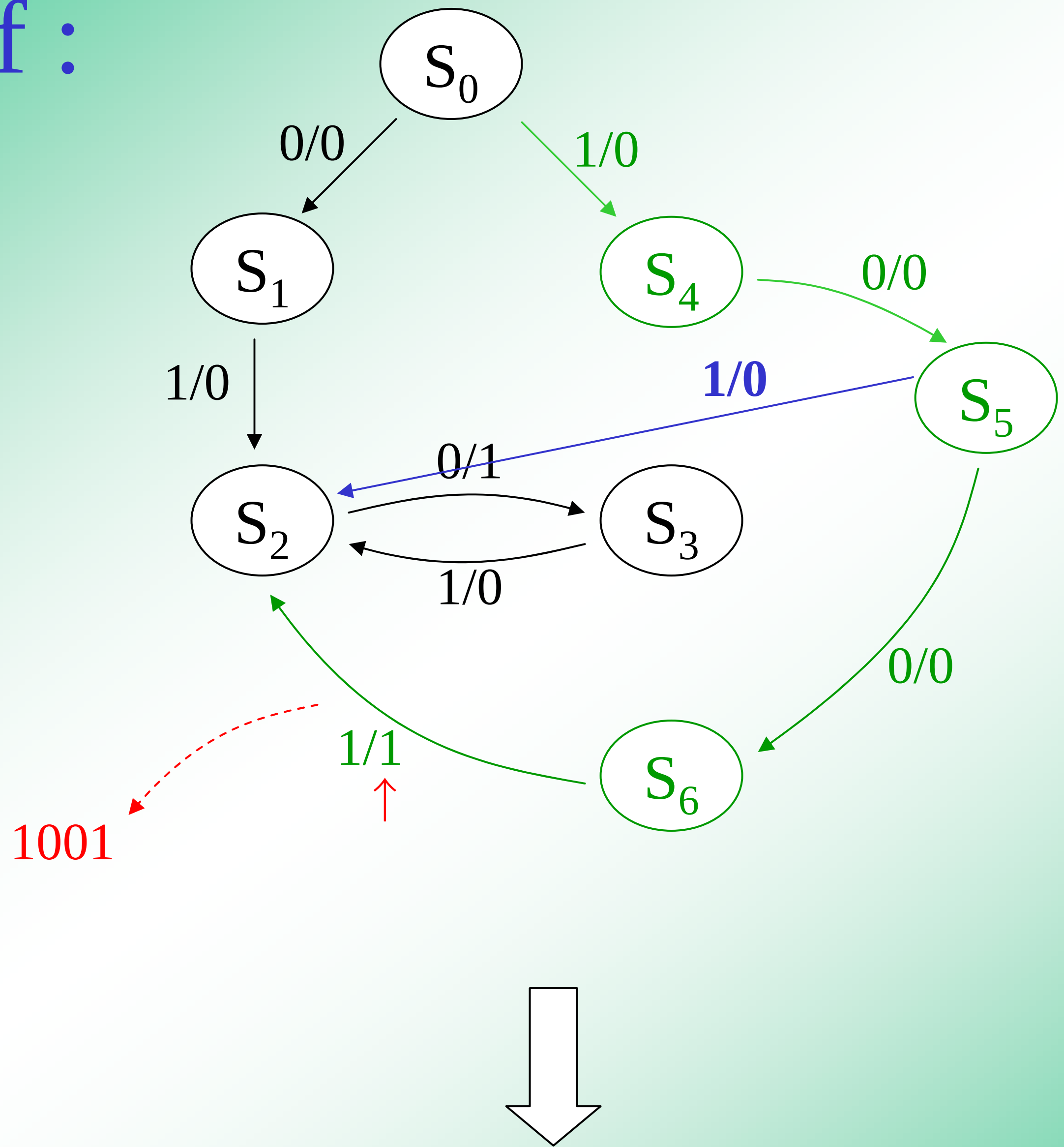
Completion of state graph



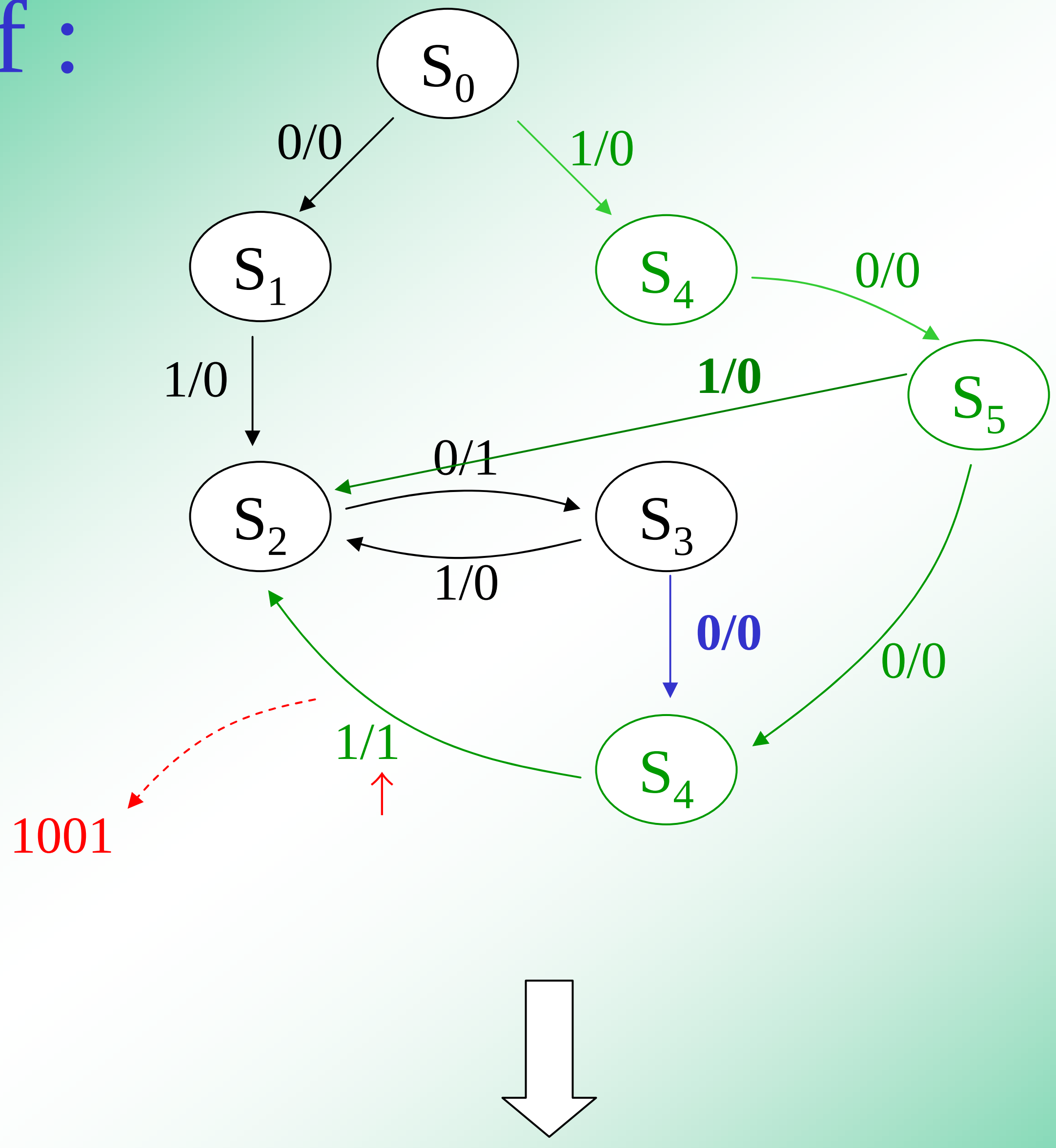
If :

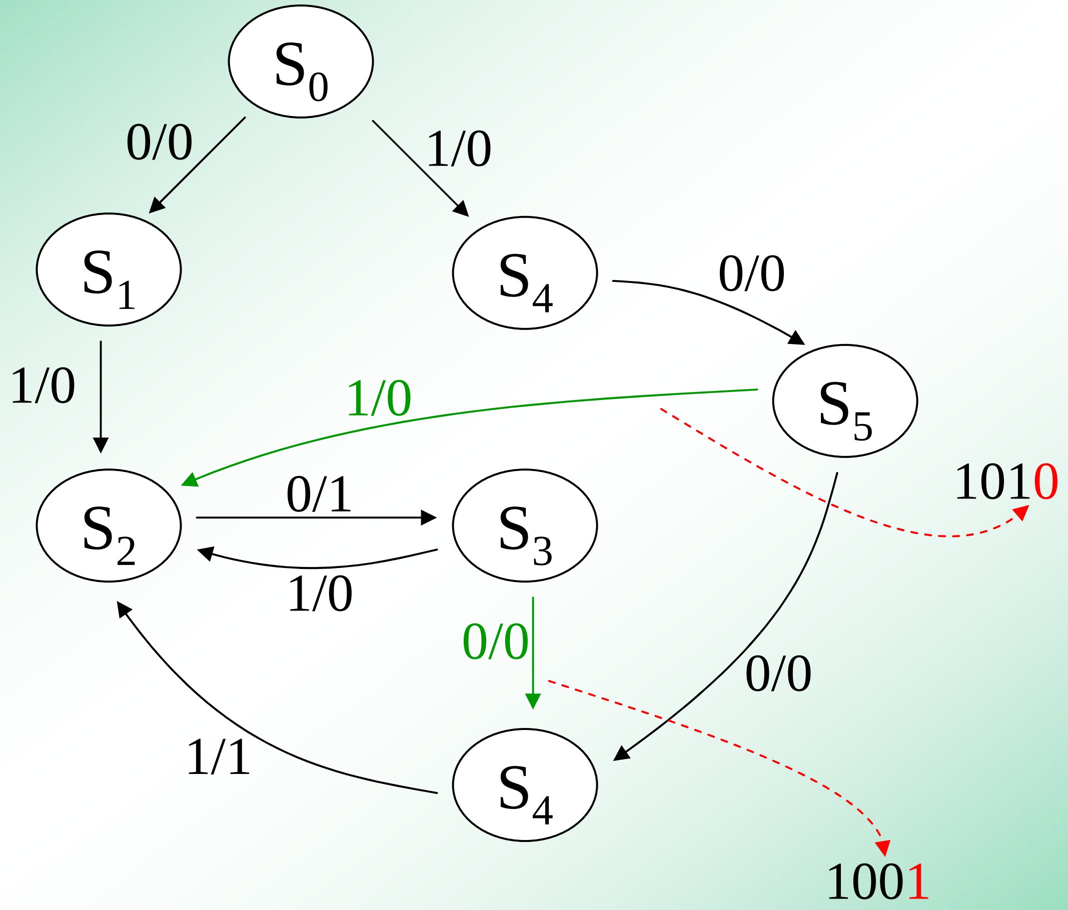


If :



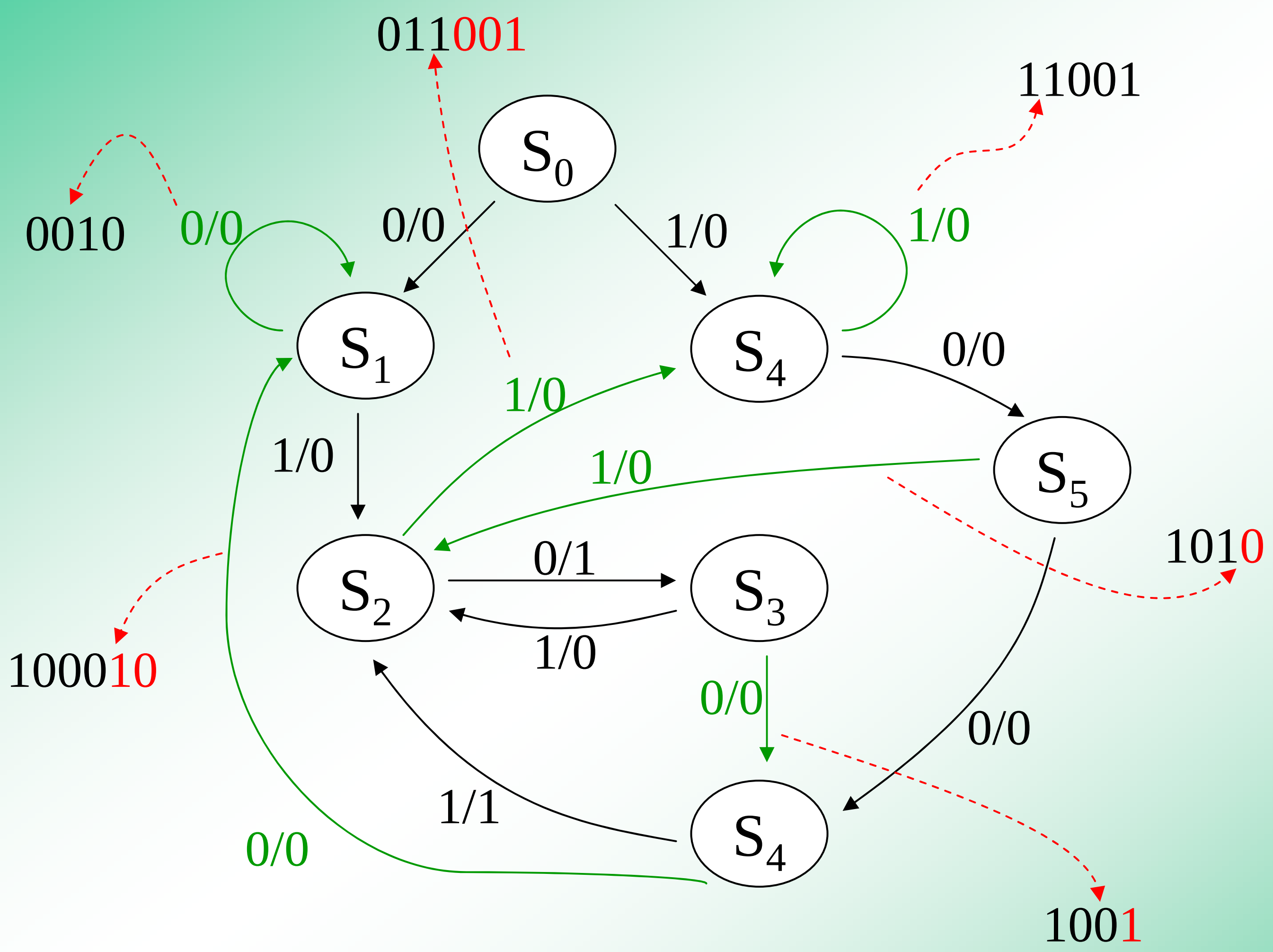
If :





S_3 , S_5 have the same next states (S_2 , S_6)

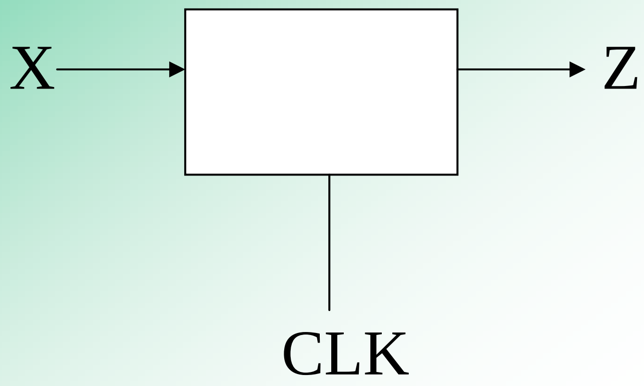
$\Rightarrow S_3 \equiv S_5$ (equivalent)



S_3 , S_5 have the same next states (S_2 , S_6)

$\Rightarrow S_3 \equiv S_5$ (equivalent)

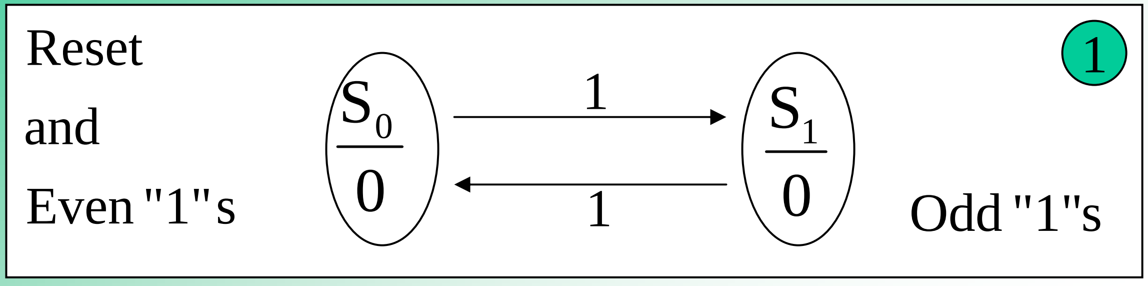
– Moore Machine Example –

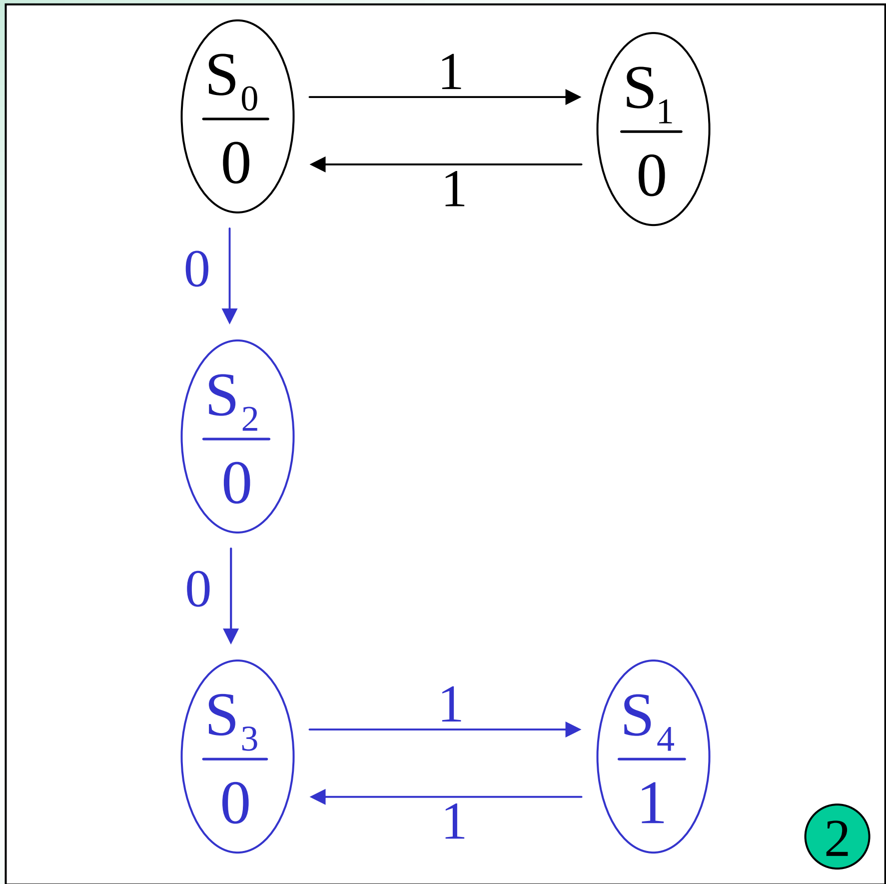


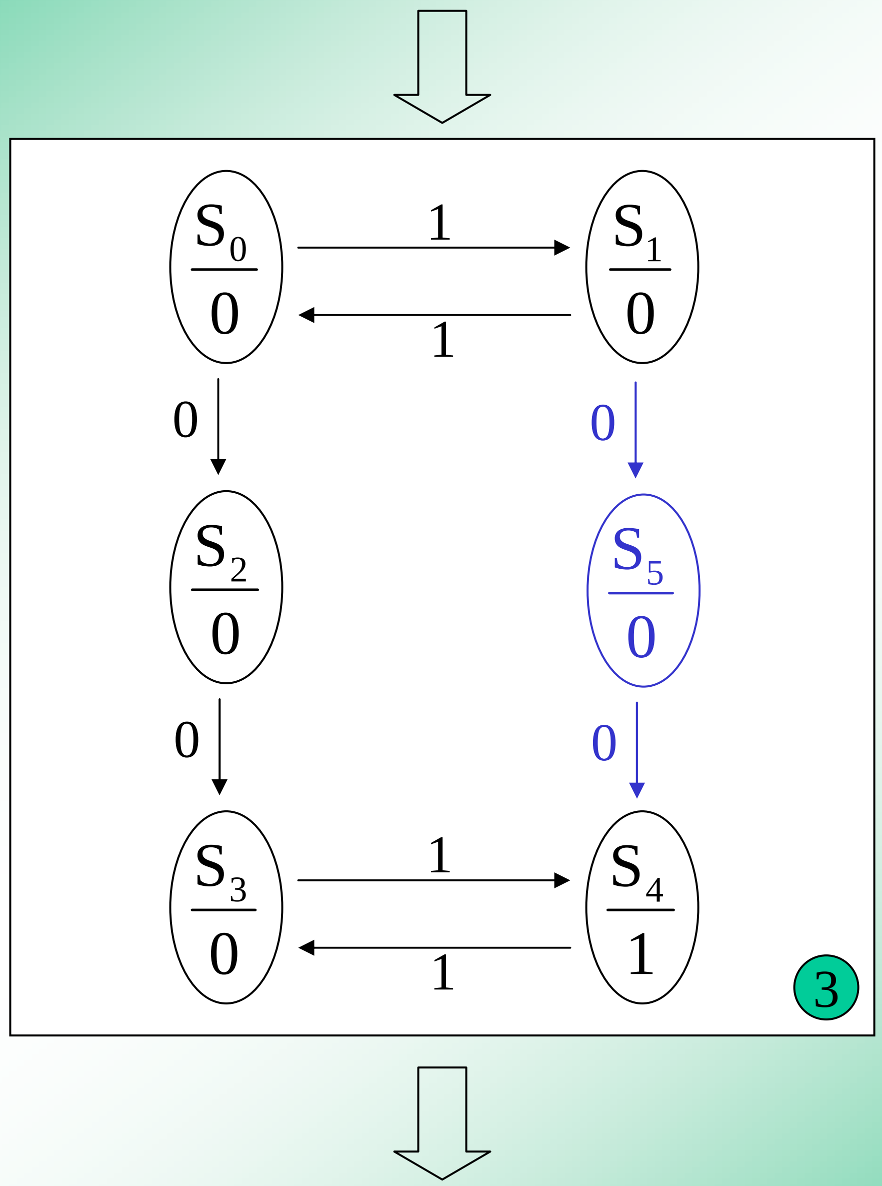
Z gives "1" if total number of "1" received is "odd" and at least 2 consecutive "0" received

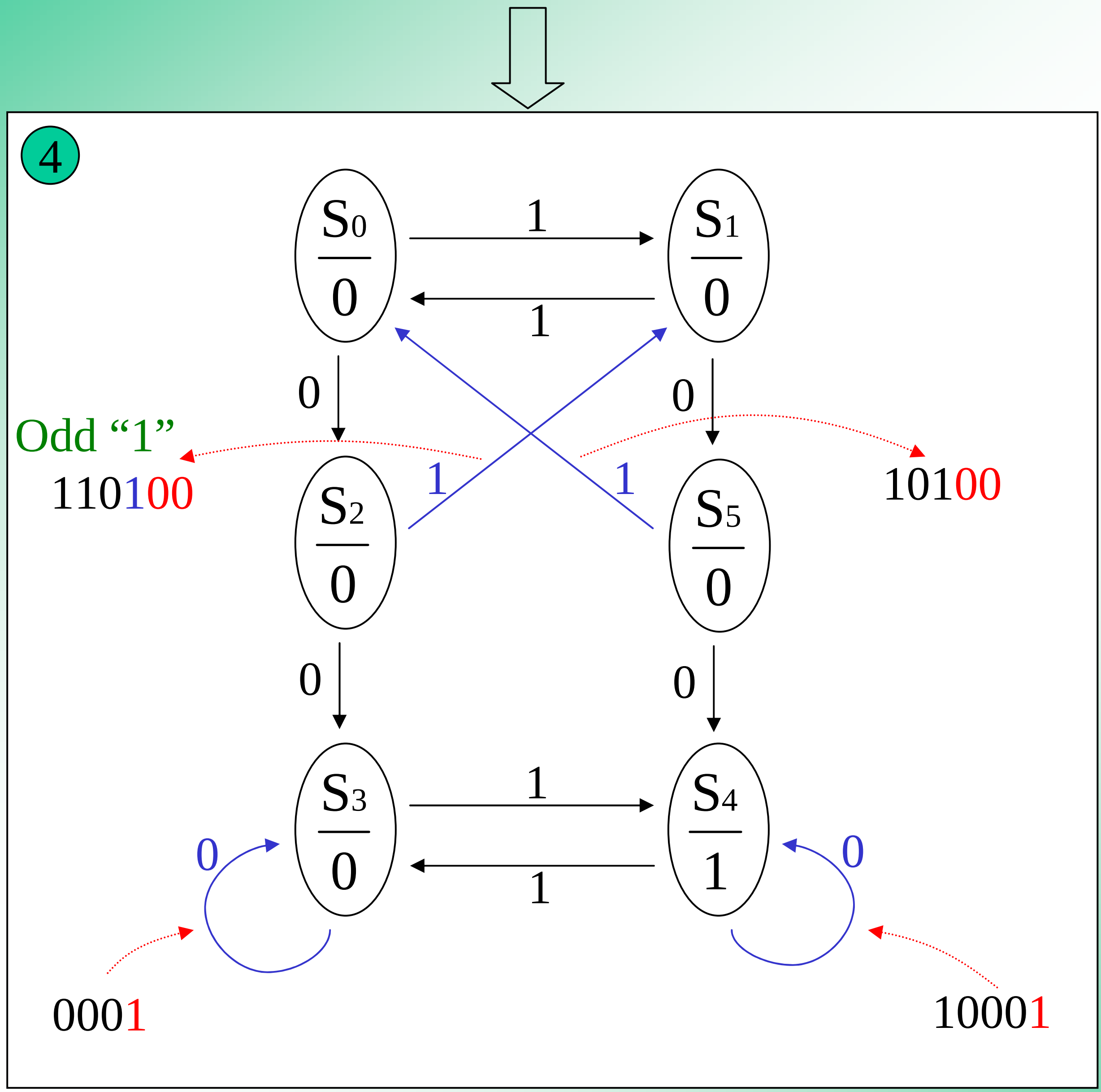
Otherwise, Z gives "0"

X	=		1	0	1	1	0	0	1	1
Z	=	(0)	0	0	0	0	0	1	0	1


Reset
and
Even "1"s
S0
0
1
1
S1
0
Odd "1"s
1

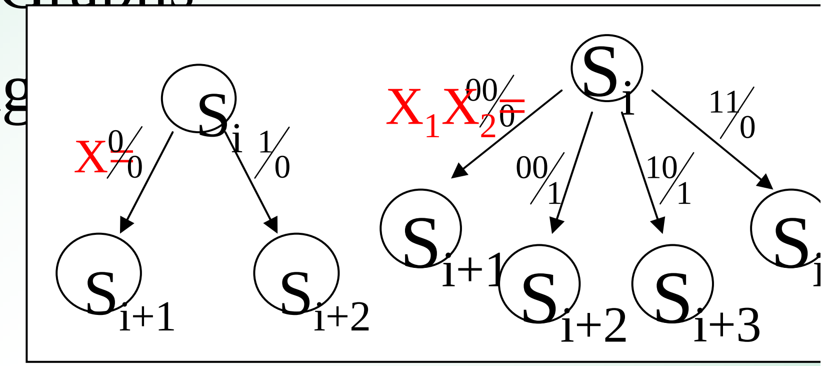

S0
0
1
1
S1
0
0
S2
0
0
S3
0
1
1
S4
1
2


S0
0
S1
0
S2
0
S5
0
S3
0
S4
1
1
1
0
0
0
0
1
1
3


4
S0
0
S1
0
S2
0
S5
0
S3
0
S4
1
1
1
1
1
0
0
0
0
1
1
0
0
Odd "1"
110100
10100
0001
10001

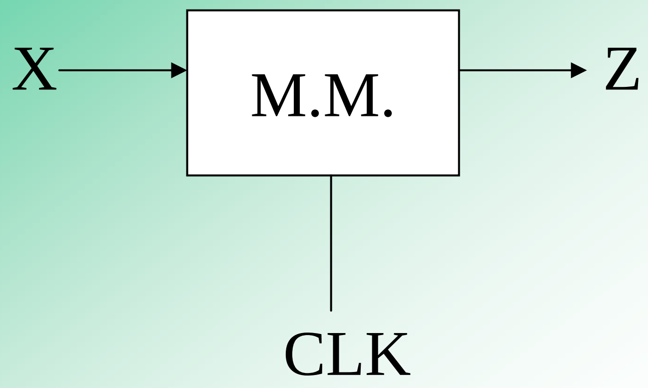
14-3 Guidelines for Construction of State Graphs

§ Guidelines for Construction of State Graphs



1. Understand problem by constructing sample sequences.
2. Determine reset state
3. Construct partial graph to obtain "1" output
4. Construct remaining partial graphs to obtain "1" output.
5. When seting up a new state , see whether it can go to an existing state.
6. Complete the graph. (Check all output 組合 !!)
7. 驗算 !!

Example : A Mealy Machine

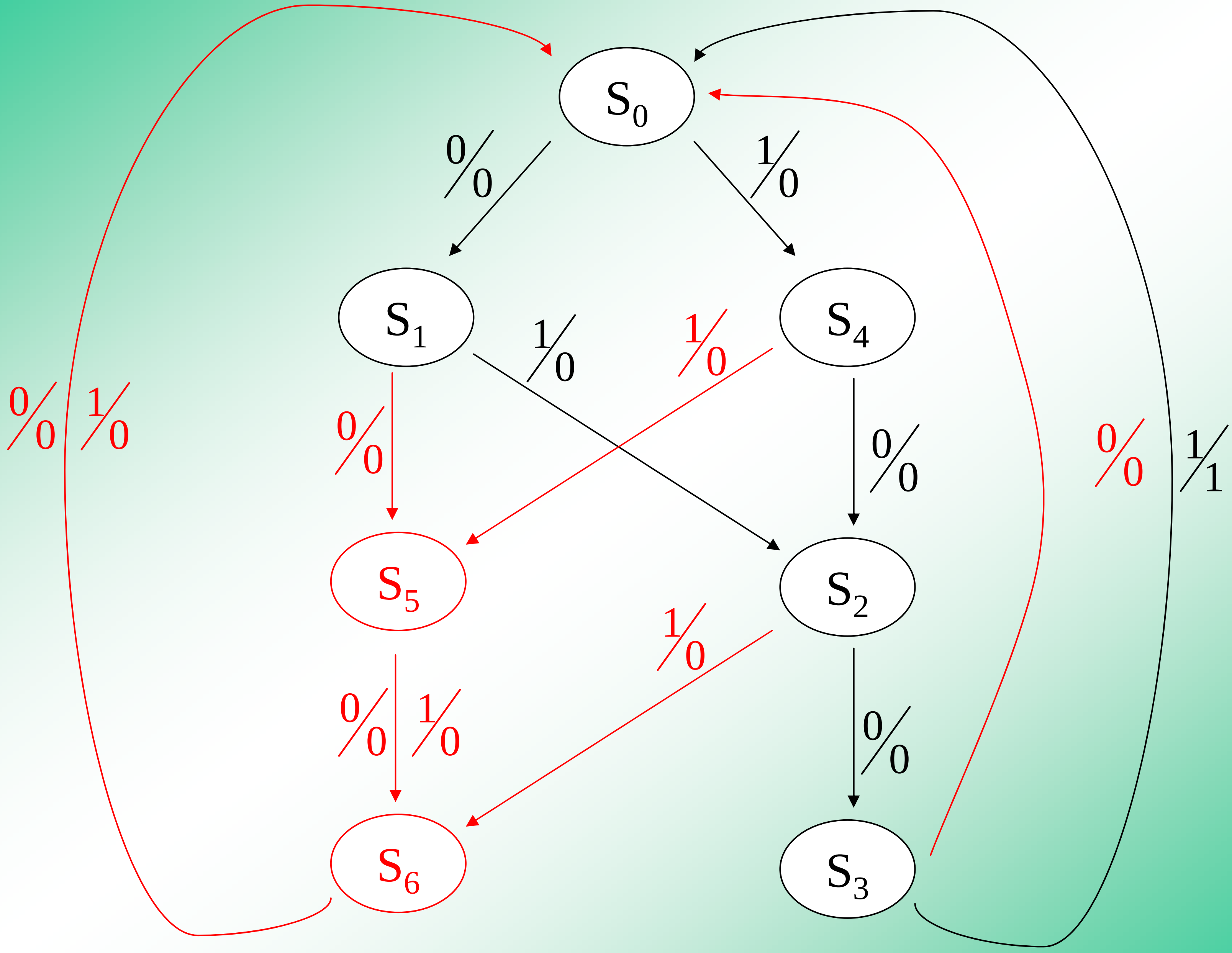


Check 4 consecutive outputs as a group , then resets

gives "1" when X = 0101 or 1001

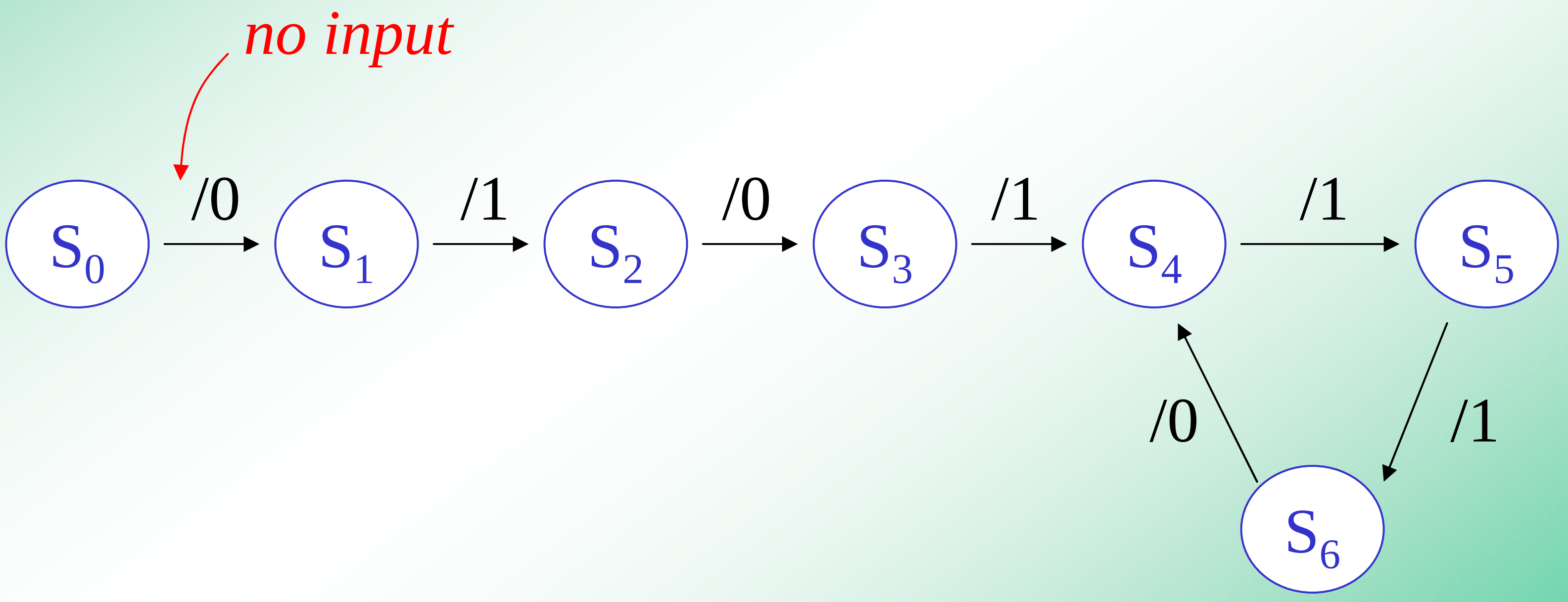
X	=	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0
Z	=	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

分析 : gives "1" if either "01" or "10" followed by "01"

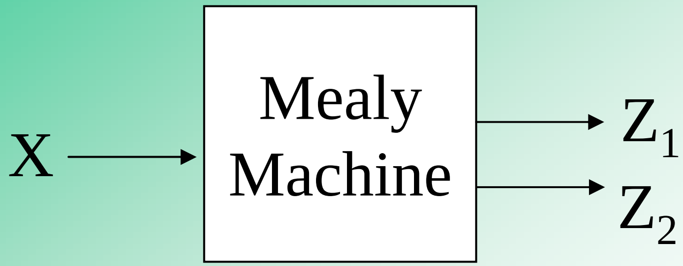

S0
0/0
1/0
S1
1/0
1/0
S4
0/0
0/0
0/0
1/0
0/0
0/0
1/1
S5
S2
1/0
0/0
1/0
0/0
S6
S3

Example:

Find the Mealy state graph for a network that generates ***0101*** ***<u>110</u>*** ***<u>110</u>*** ***<u>110</u>***

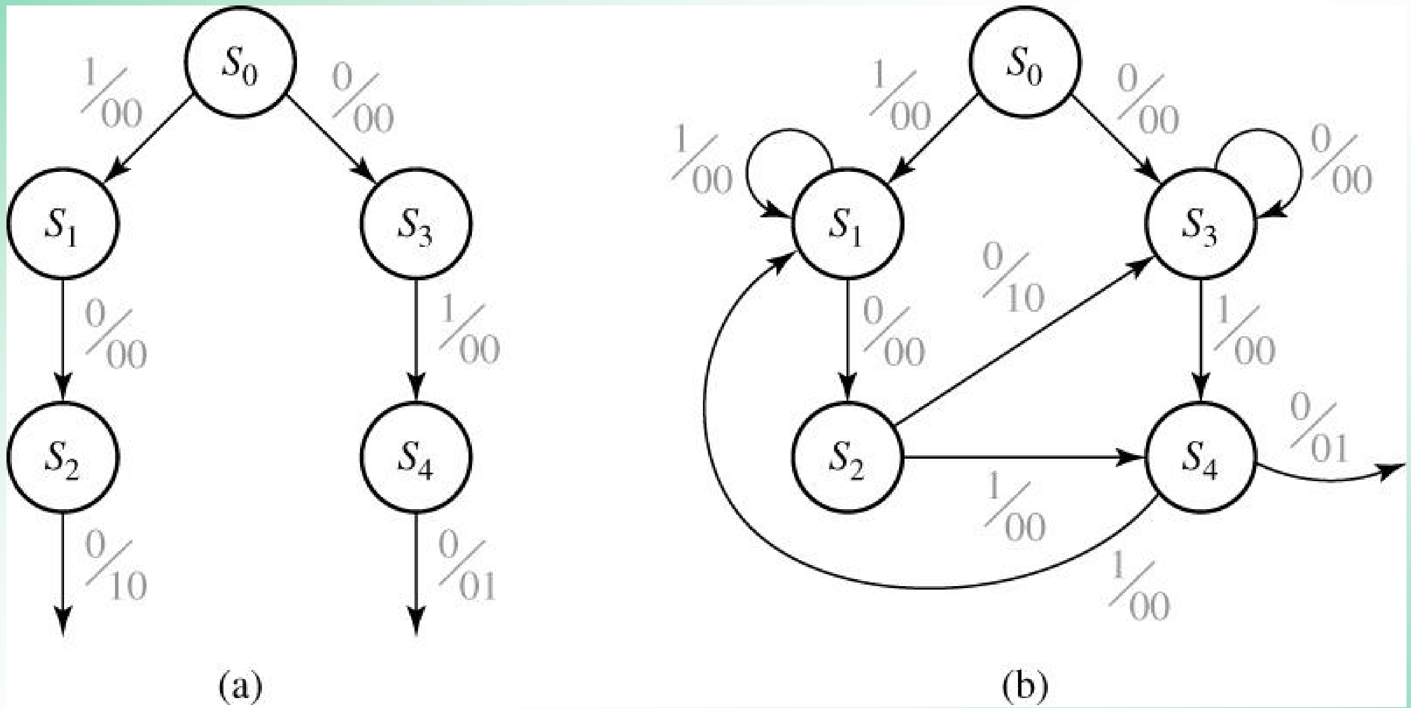


Example:

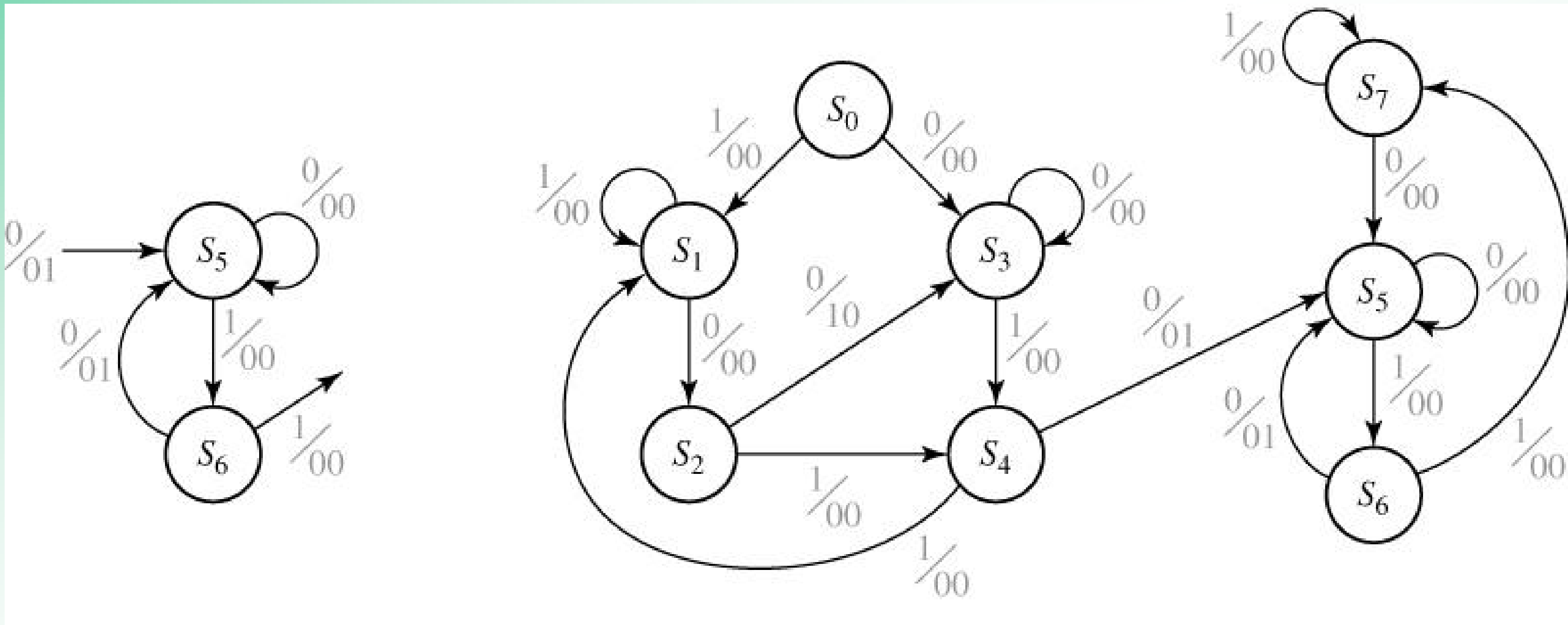


Z_1=1 if sequence 100 occurs,
Assume 010 has never occurred
Z_2=1 if sequence 010 occurs,
Note. Once a Z_2 =1, Z_1 =1 never occur.
But not vice versa

X1 = 1 0 0 1 1 0 0 1 0 | 1 0 1 0 0 1 0 1 1 0 1 0 0
Z1 = 0 0 1 0 0 0 1 0 0 | 0 0 0 0 0 0 0 0 0 0 0 0 0
Z2 = 0 0 0 0 0 0 0 0 1 | 0 1 0 1 0 0 1 0 0 0 0 1 0

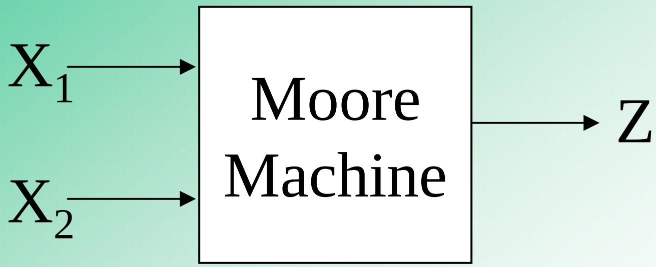


S_0
S_1
S_2
S_3
S_4
1/00
0/00
0/10
1/00
0/01
(a)
S_0
S_1
S_2
S_3
S_4
1/00
0/00
0/10
1/00
0/01
(b)



(a) Partial graph for 010 (b) Complete state graph

Example:



Z remains a constant value ("0" or "1") unless the following input occurs.

$X_1X_2 = 01, 11 \quad Z = 0$

$10, 11 \quad Z = 1$

$10, 01 \quad$ Z changes value

Previous inputs (x_1x_2)	Output (Z)	State Designation
00 or 11	0	S_0
00 or 11	1	S_1
01	0	S_2
01	1	S_3
10	0	S_4
10	1	S_5

Z remains a constant value ("0" or "1") unless the following input occurs.

$X_1X_2 = 01, 11 \quad Z = 0$

$10, 11 \quad Z = 1$

$10, 01 \quad Z$ changes value

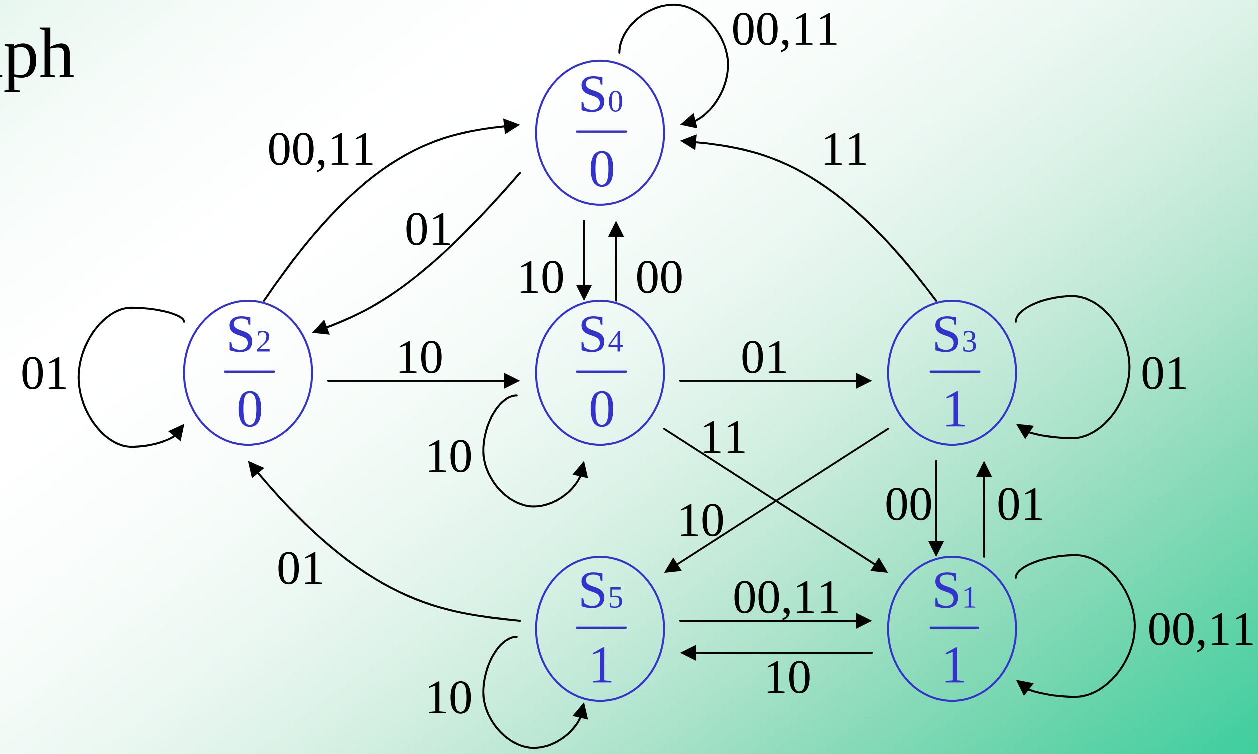
Previous inputs (x_1x_2)	Output (Z)	State Designation
00 or 11	0	S_0
00 or 11	1	S_1
01	0	S_2
01	1	S_3
10	0	S_4
10	1	S_5

P.S.	Z	x_1x_2 = 00	01	11	10
S_0	0	S_0	S_2	S_0	S_4
S_1	1	S_1	S_3	S_1	S_5
S_2	0	S_0	S_2	S_0	S_4
S_3	1	S_1	S_3	S_0	S_5
S_4	0	S_0	S_3	S_1	S_4
S_5	1	S_1	S_2	S_1	S_5

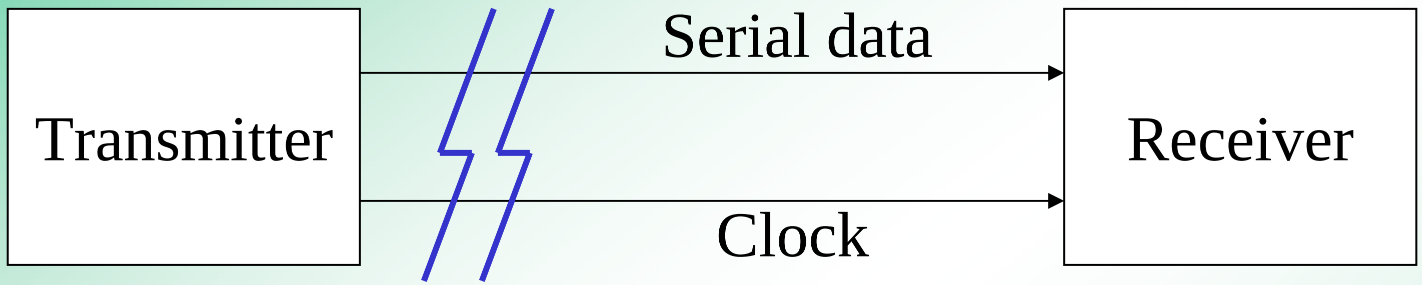
⇒ State table

P.S.	Z	x_1x_2 = 00	01	11	10
S_0	0	S_0	S_2	S_0	S_4
S_1	1	S_1	S_3	S_1	S_5
S_2	0	S_0	S_2	S_0	S_4
S_3	1	S_1	S_3	S_0	S_5
S_4	0	S_0	S_3	S_1	S_4
S_5	1	S_1	S_2	S_1	S_5

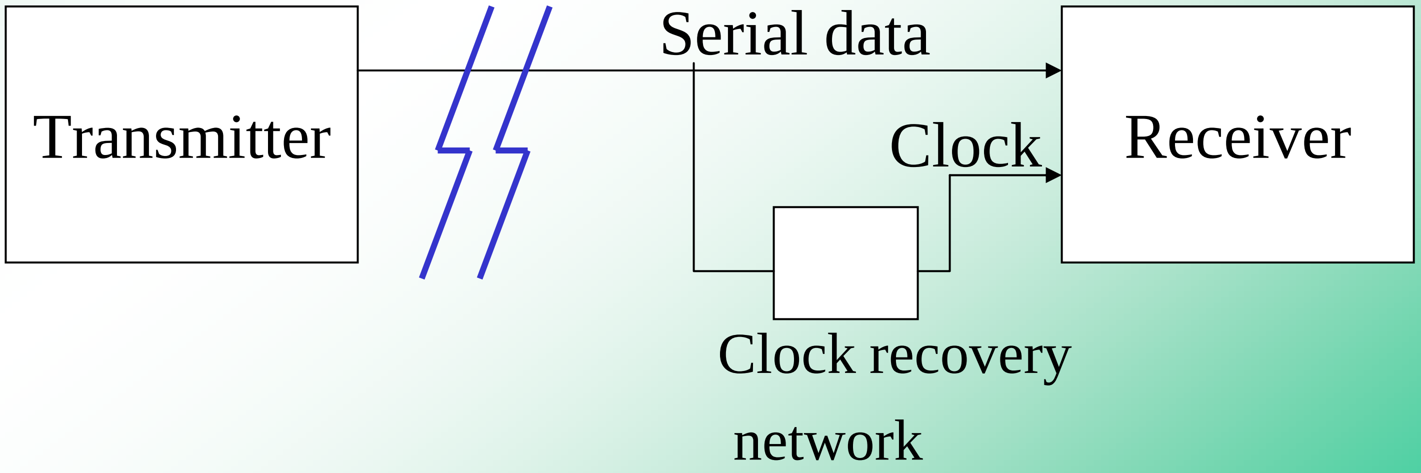
* State graph



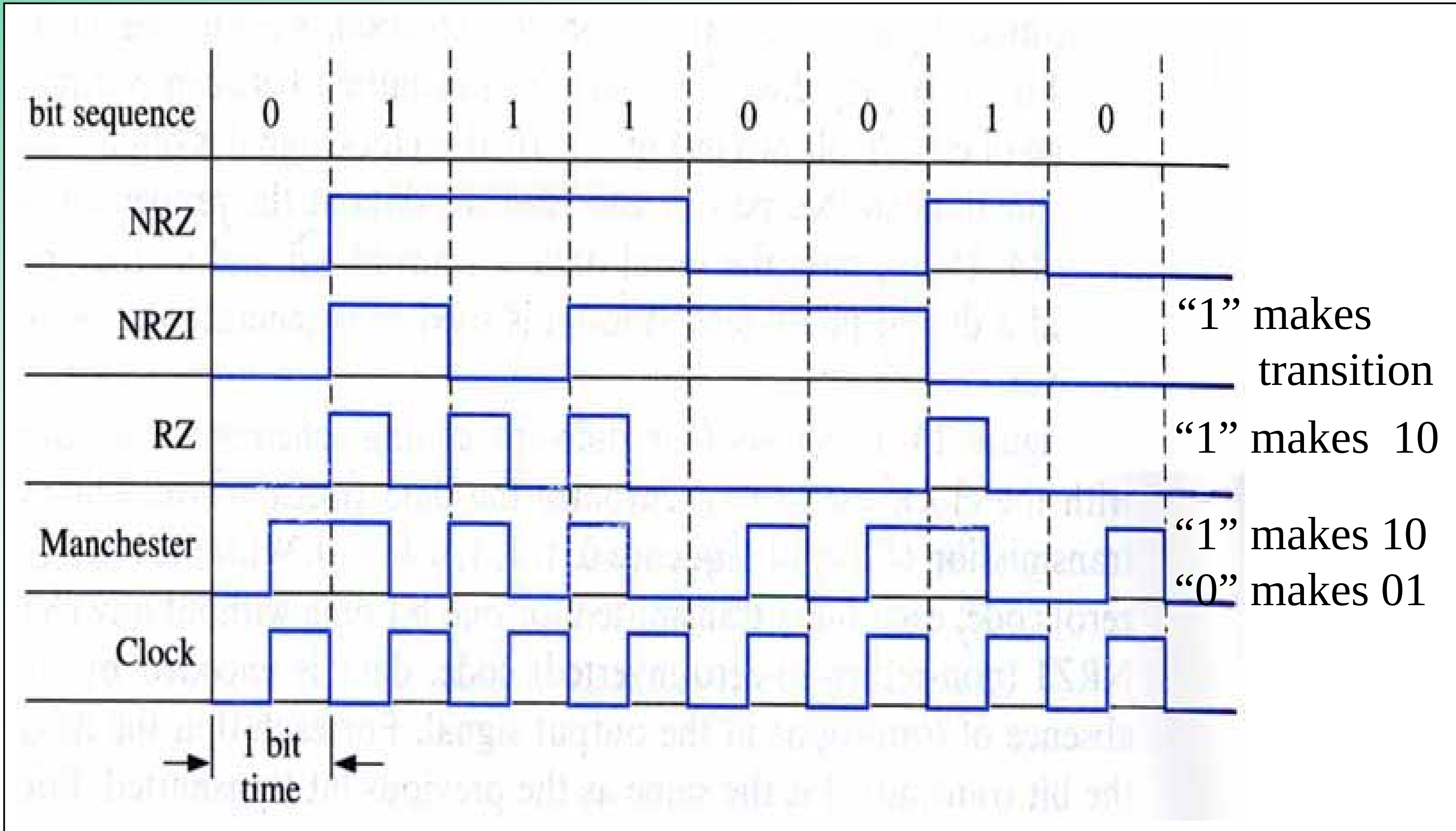
14-4 Serial Data Code Conversion

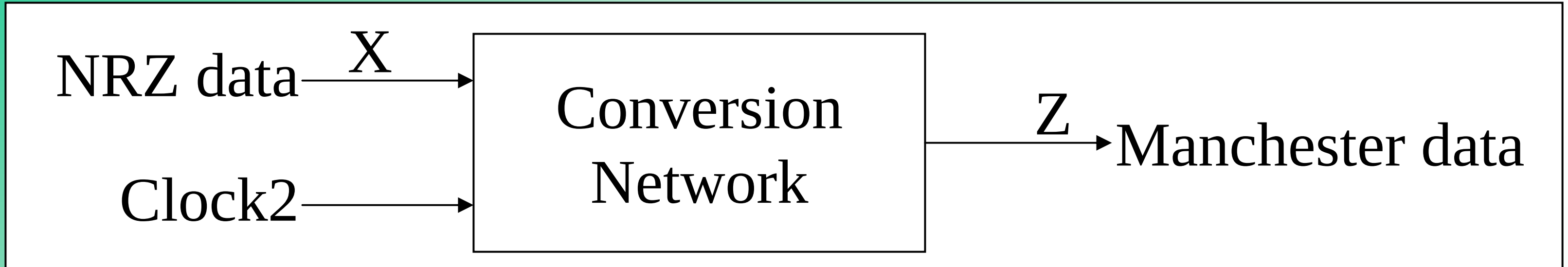


Use 2 cables (not good)

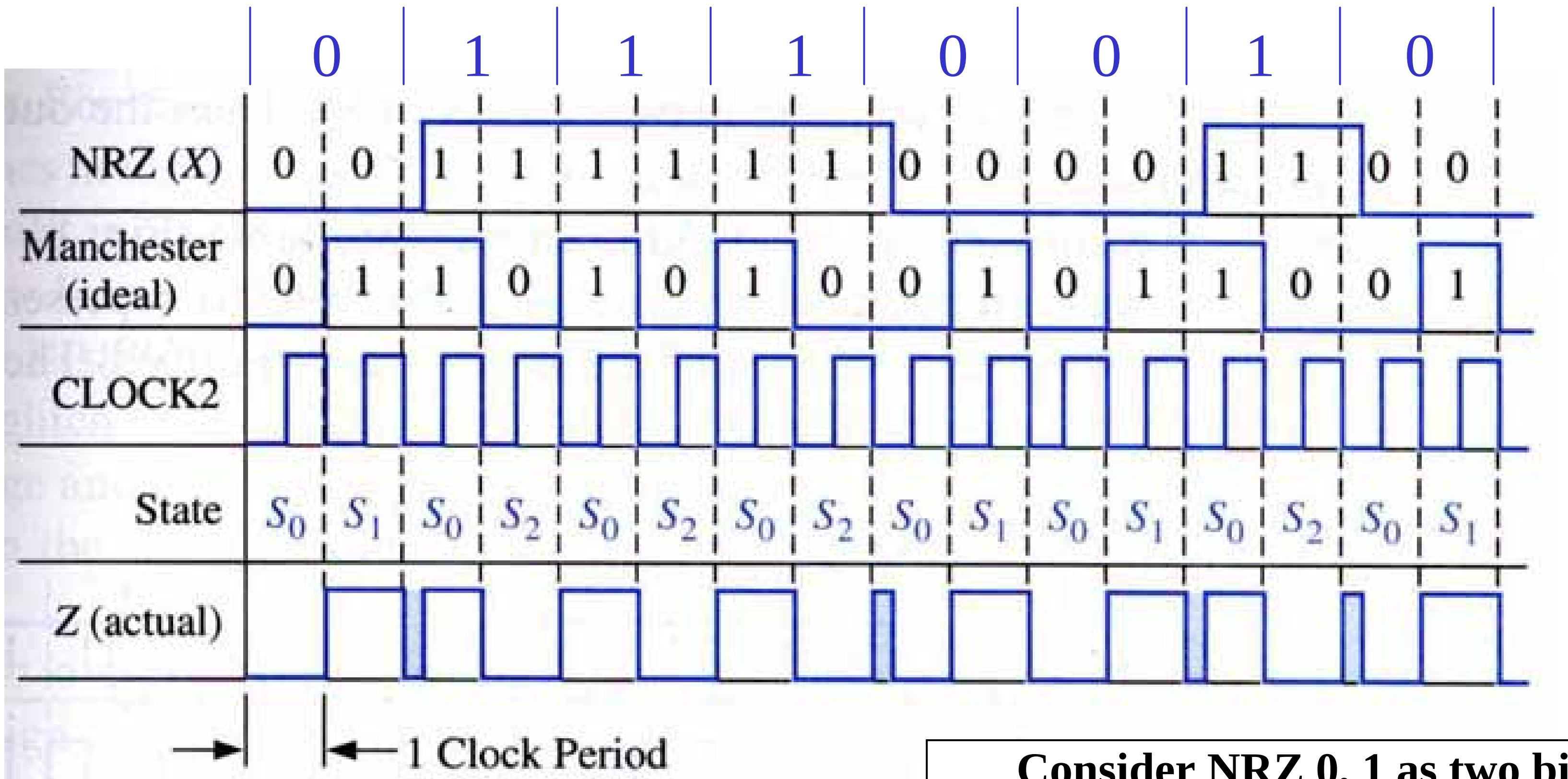


*Coding schemes





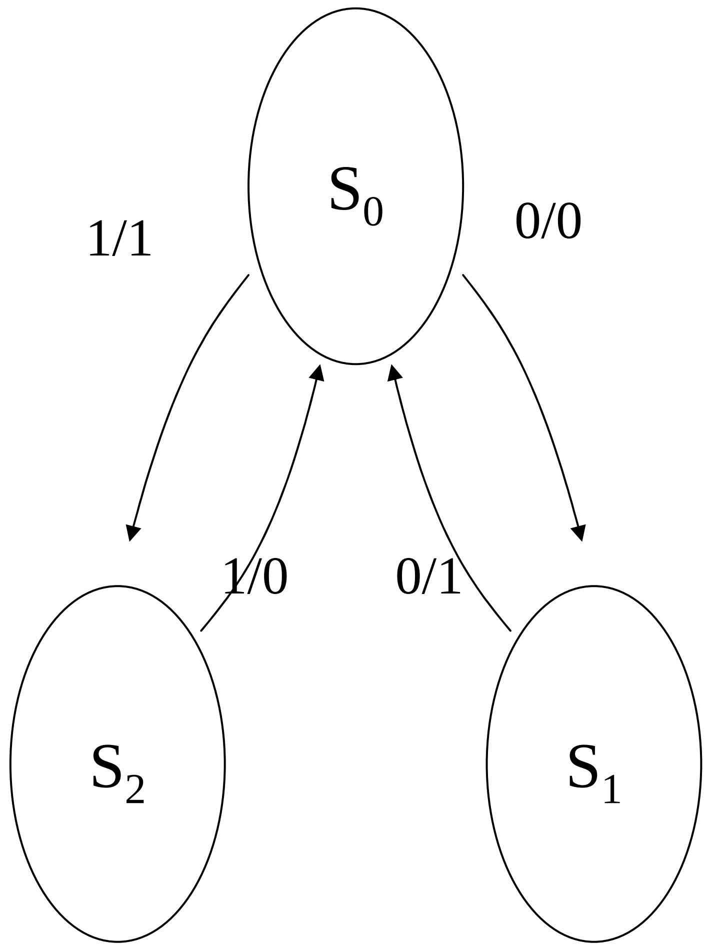
(a)Conversion network



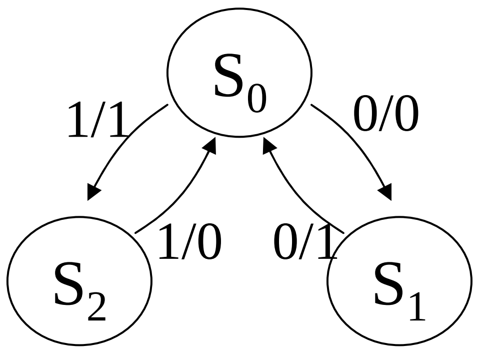
(b)Timing Chart

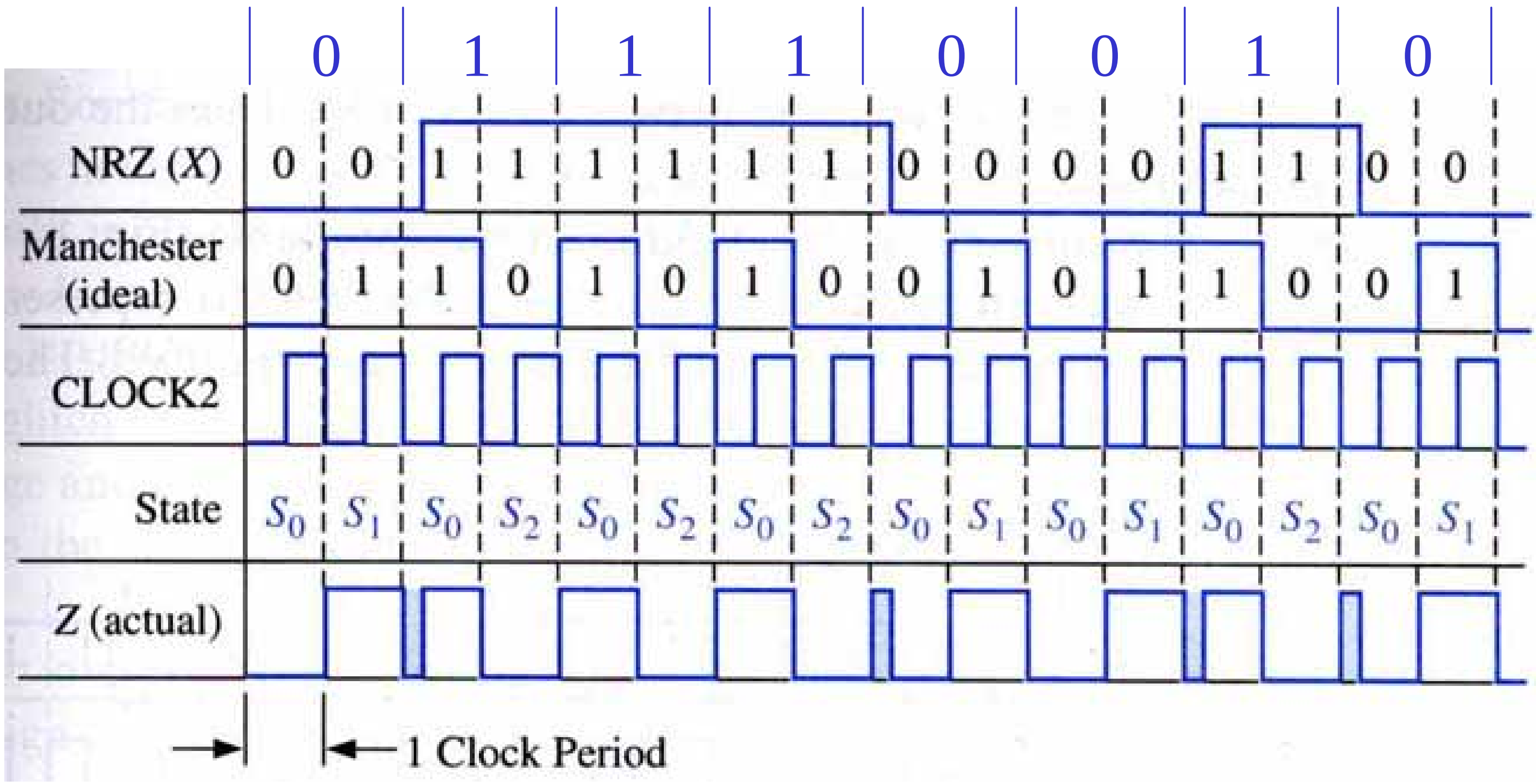
Consider NRZ 0, 1 as two bits which occur consecutively! Every two bits, machine returns to reset state

(c)State graph



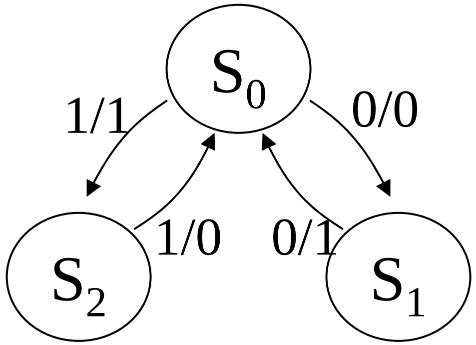
(c)State graph





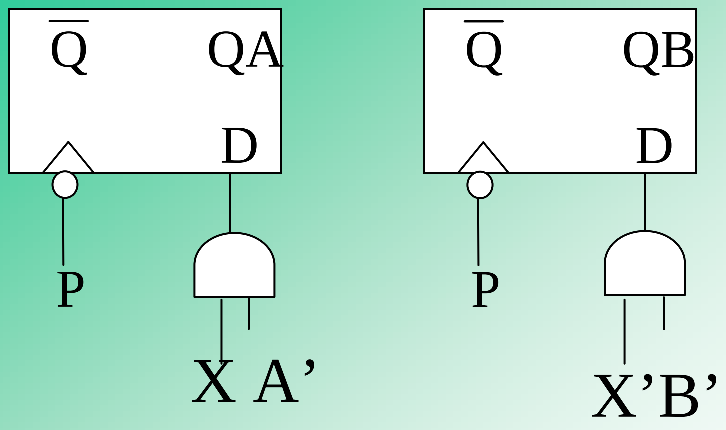
(b)Timing Chart

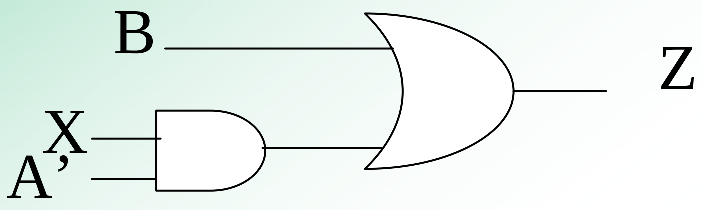
(c)State graph



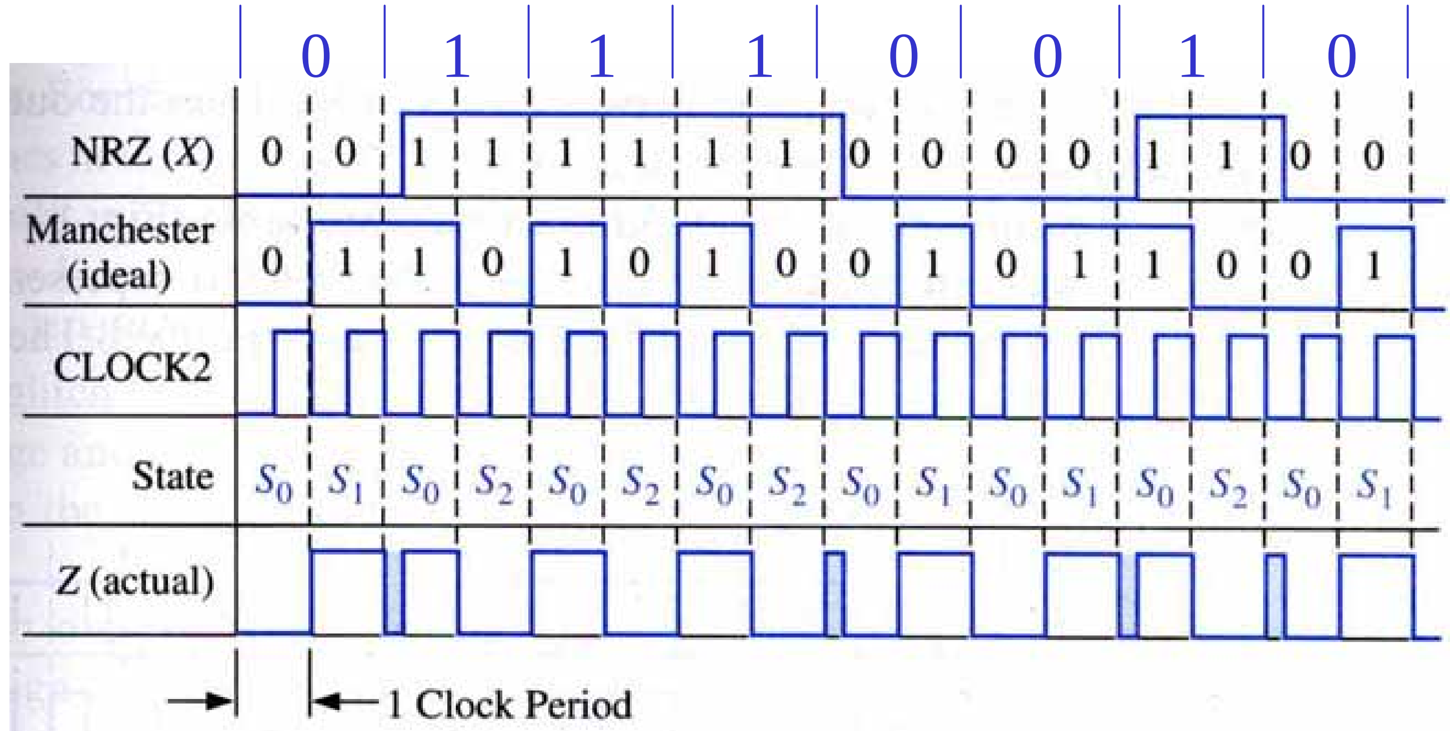
Present state	Nest state $x=0$	Nest state $x=1$	Output (Z) $x=0$	Output (Z) $x=1$
S_0	S_1	S_2	***0***	***1***
S_1	S_0	–	***1***	–
S_2	–	S_0	–	***0***

(d)State table



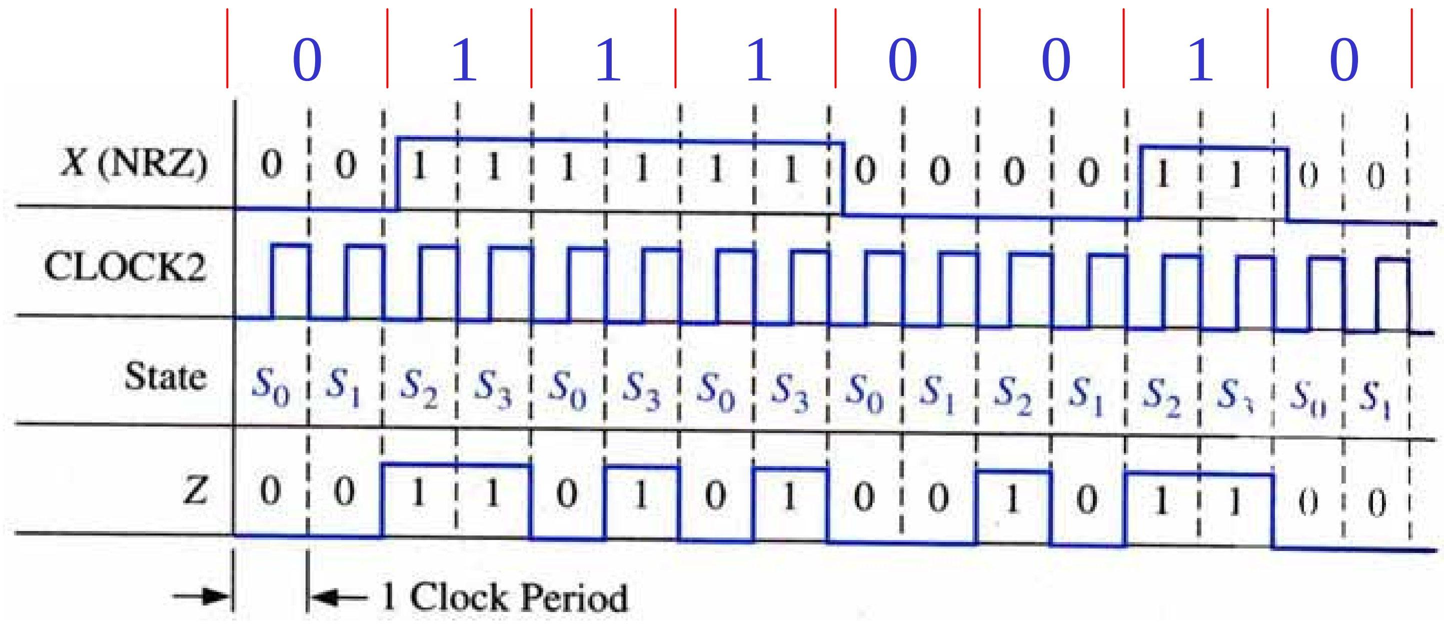


S0	AB = 00	X=0 , Z=0	X=1, Z=1
S1	10	X=0 , Z=0	X=1, Z=0
S2	01	X=0, Z= 0	X=1, Z=1

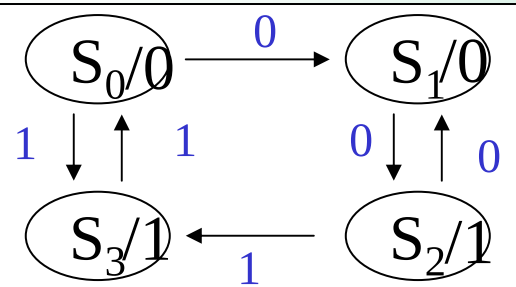


(b)Timing Chart

*Moore Machine



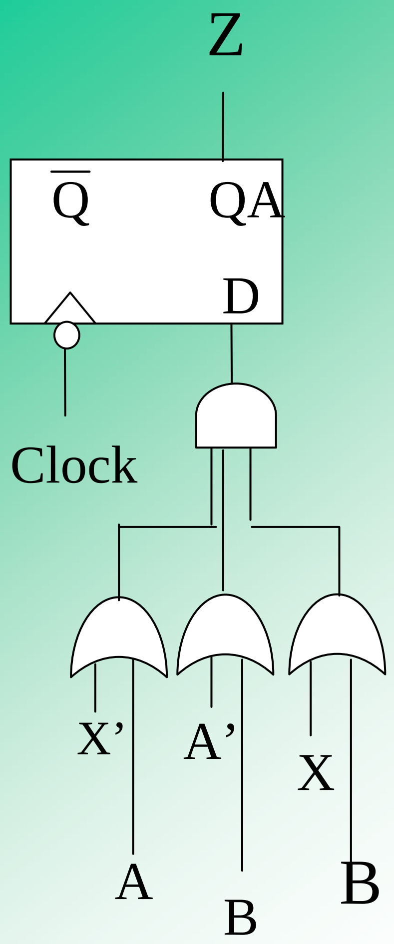
(a)Timing Chart



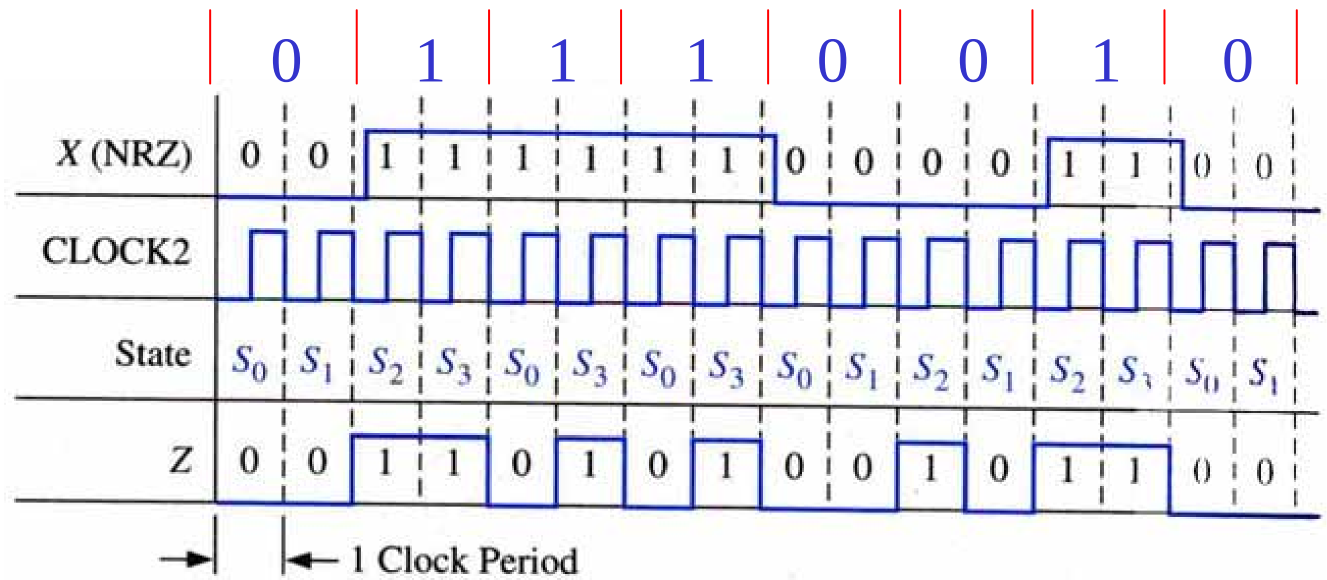
(b)State graph

Present state	Nest state $x=0$	$x=1$	Present Output (Z)
S_0	S_1	S_3	***0***
S_1	S_2	$-$	***0***
S_2	S_1	S_3	***1***
S_3	$-$	S_0	***1***

(C)State table



S0 AB = 00
S1 01
S2 11
S3 10

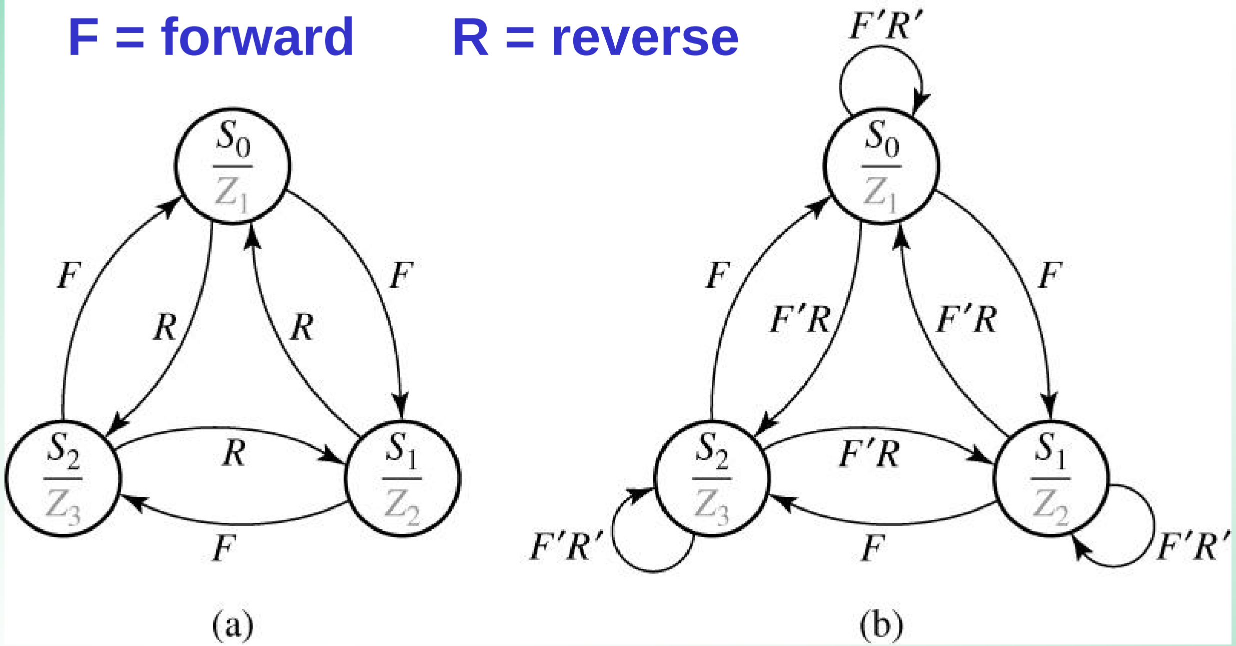


(a)Timing Chart

14-5 Alphanumeric State Graph Notation

- When a state sequential circuit has several inputs,
  - Label the state graph arcs with alphanumeric input variable

F = forward **R = reverse**



not complete

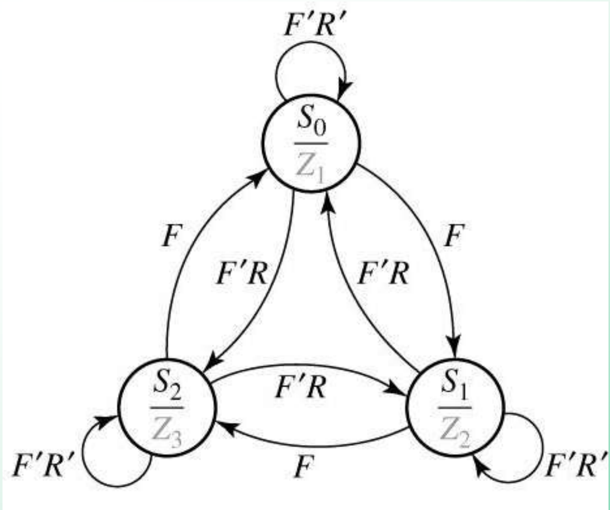
PS	NS					Output		
	FR=	00	01	10	11	Z_1	Z_2	Z_3
S_0		S_0	S_2	S_1	S_1	1	0	0
S_1		S_1	S_0	S_2	S_2	0	1	0
S_2		S_2	S_1	S_0	S_0	0	0	1

- **Property of the complete specified state graph**
  - **OR** together all input labels on arcs emanating from a state, the result can reduce to 1

$$F + F'R + F'R' = F + F' = 1$$

  - **AND** together any pair of input labels on arcs emanating from a state, the result can reduce to 0

$$F \cdot F'R = 0, \quad F \cdot F'R' = 0, \quad F'R \cdot F'R' = 0$$



- For large sequential circuits (4 inputs, 4 outputs)
  - X_1X_4'/Z_2Z_3 1--0/0110
  - $-/Z_1$ for any combination of input values, the indicated state will occur and output Z_1=1

HOMEWORK -- Unit 14

- 14.07(a)
- 14.17
- 14.21
- 14.31