Chap 11: Flip-Flops

Combinational: Output is a function of present inputs only

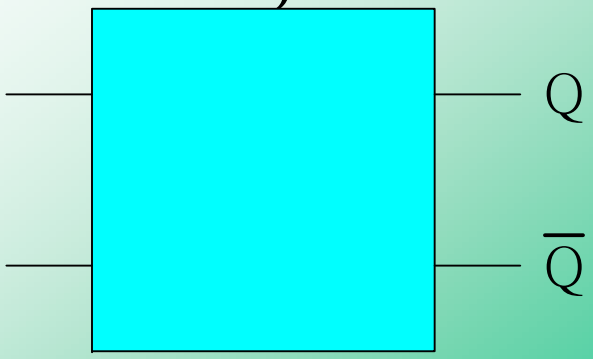
Sequential : Output is function both present and previous inputs

Circuit "remembers" previous history

→ Flip Flop (F/F): with clock input (on clock edge)

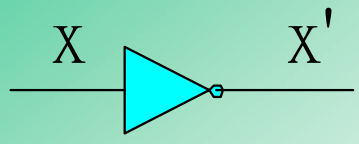
→ Latches : with no clock input (on clock level)

F/F: a memory device with 1 output, or 2 complementary outputs

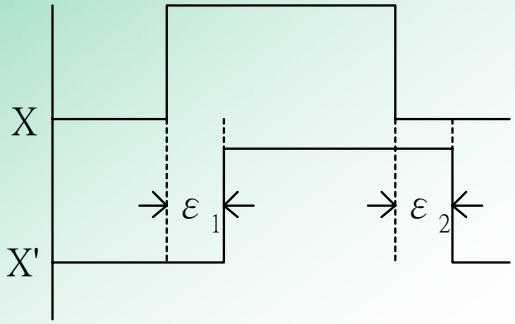


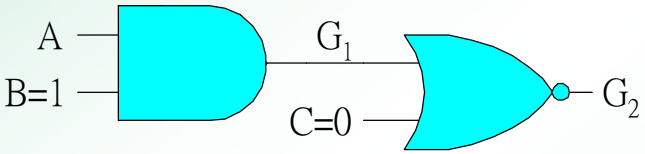
Timing in combinational circuits

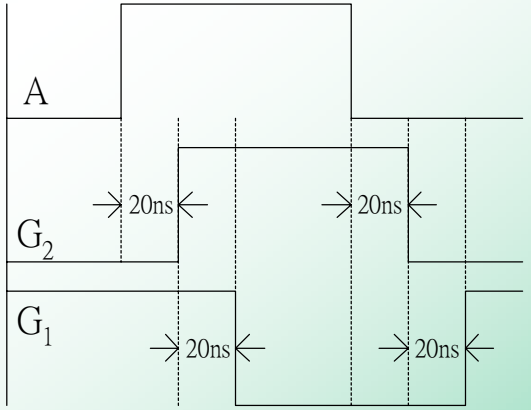
That's what we learn up to now.

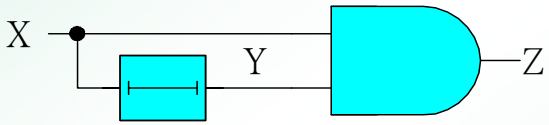


ε_1, ε_2 may be very small but still exist.

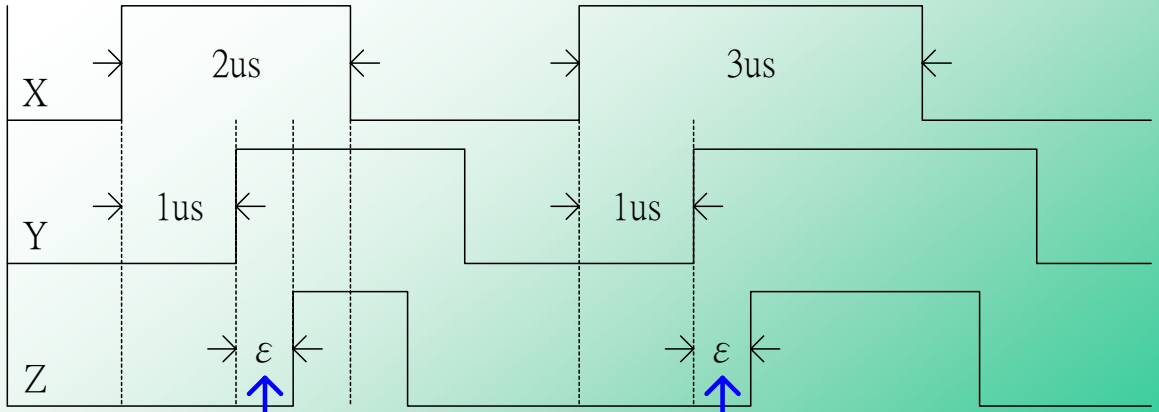








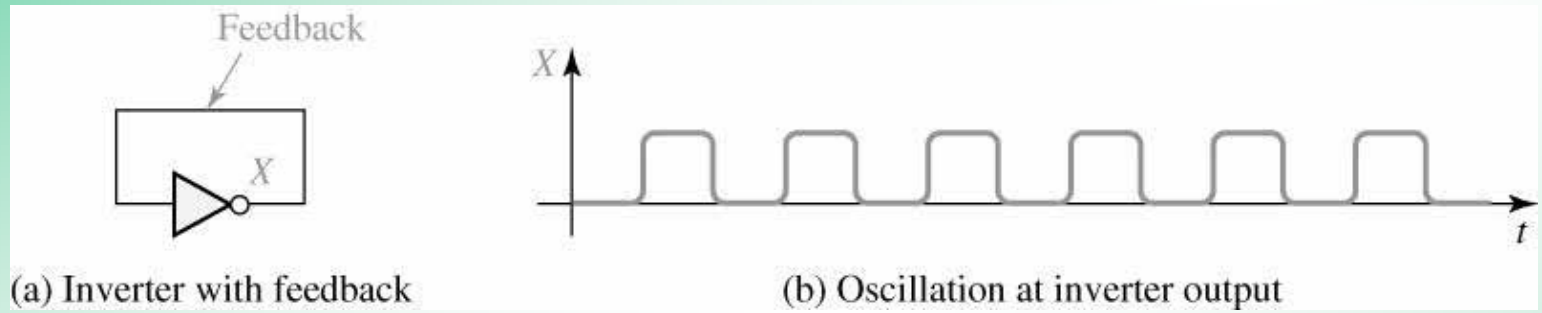
1us delay
due to wire lenth



How your construct a switching circuit with memory? By feedback

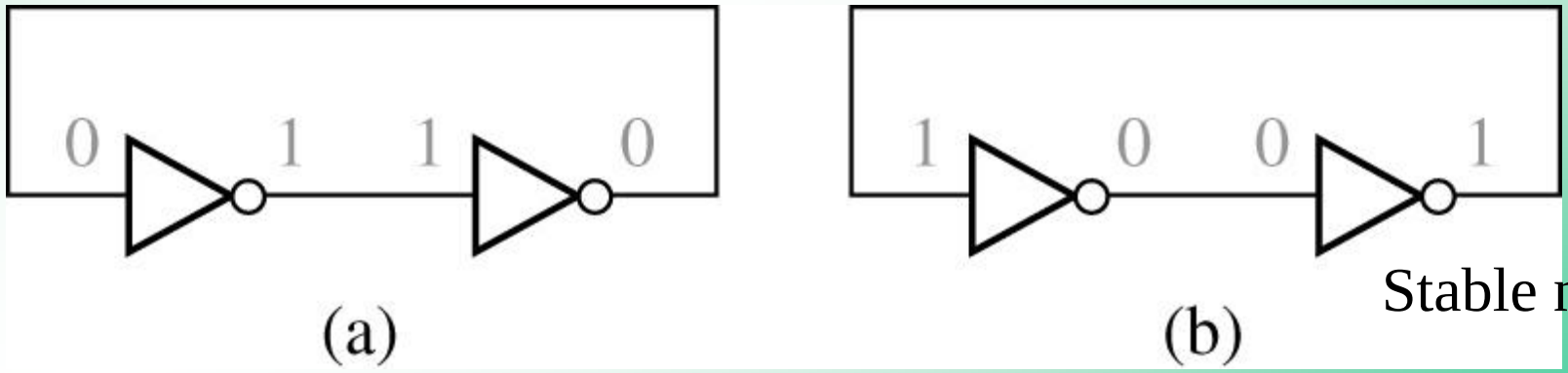
Timing in feedback Network

One inversion



(a) Inverter with feedback (b) Oscillation at inverter output

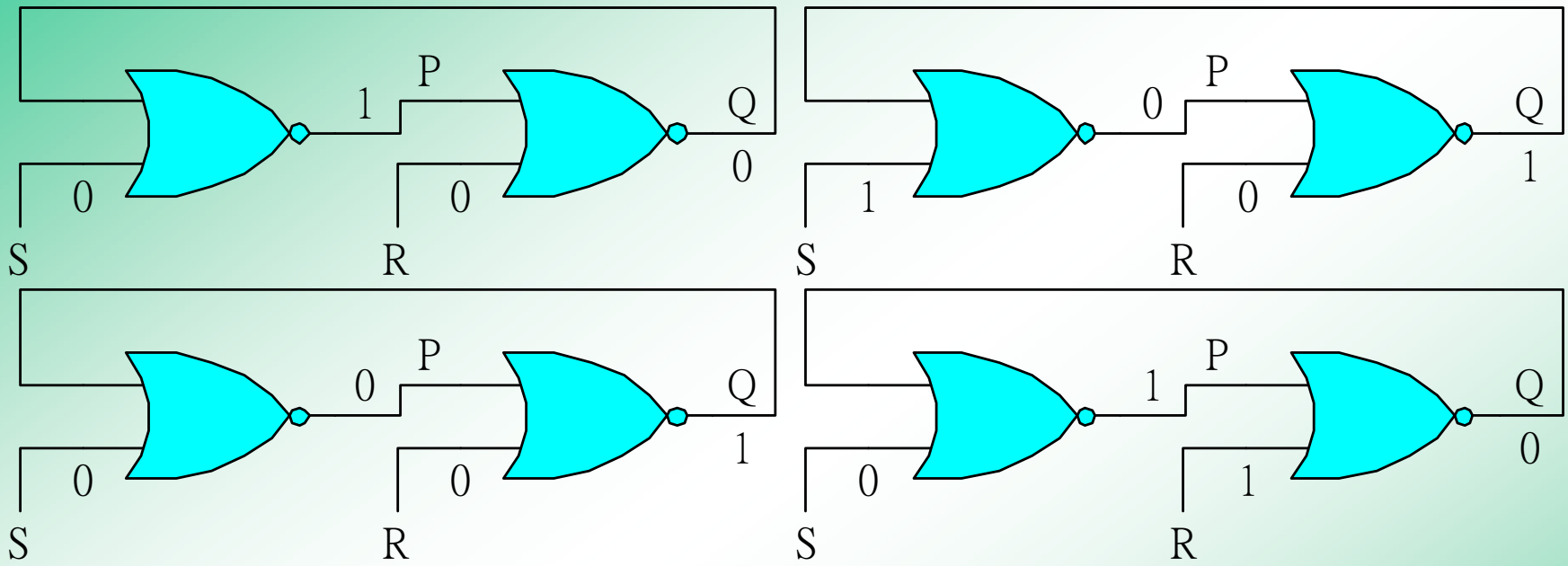
Two inversions

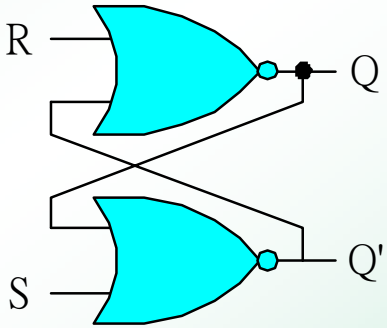


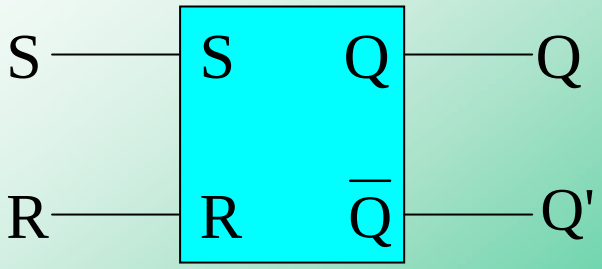
Stable now

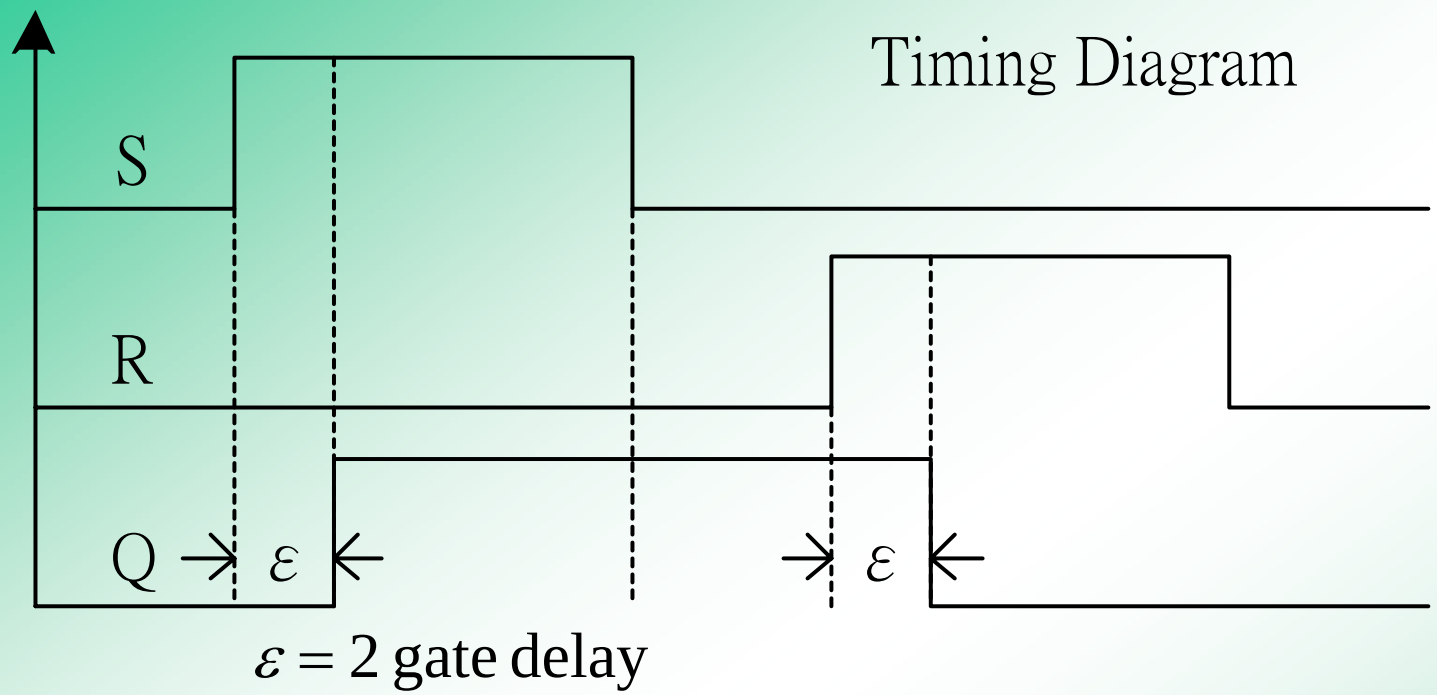
To control the stable states

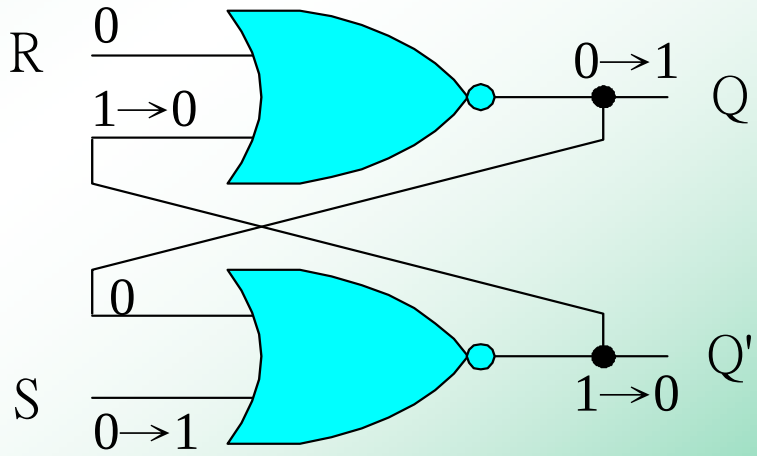
Set-Reset Latch (SR latch)








Timing Diagram
S
R
Q
ε
ε
ε = 2 gate delay


R
0
1→0
0→1
Q
0
S
0→1
1→0
Q'

if R, S 同時 $1 \rightarrow 0$,

$\Rightarrow Q = Q' = 1 \rightarrow 0$ (not allowed)

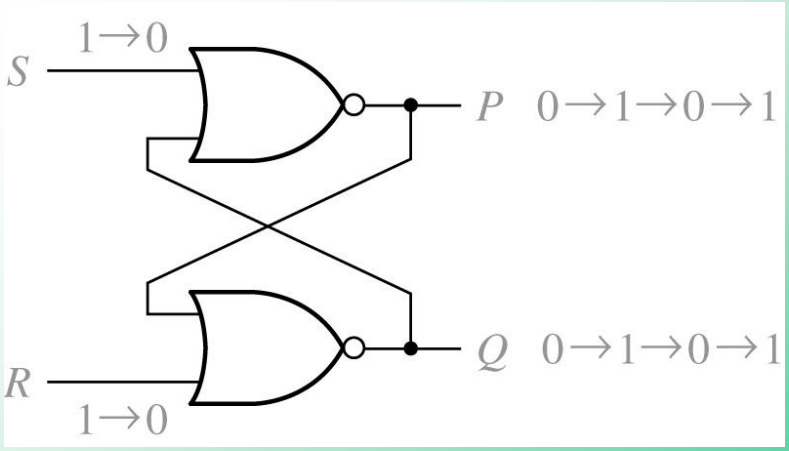
or Q = 1 first or Q' = 1 first (undetermined)

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\varepsilon)$ $(= Q^+(t))$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	–
1	1	1	–

$Q_t(Q_n)$: Present State

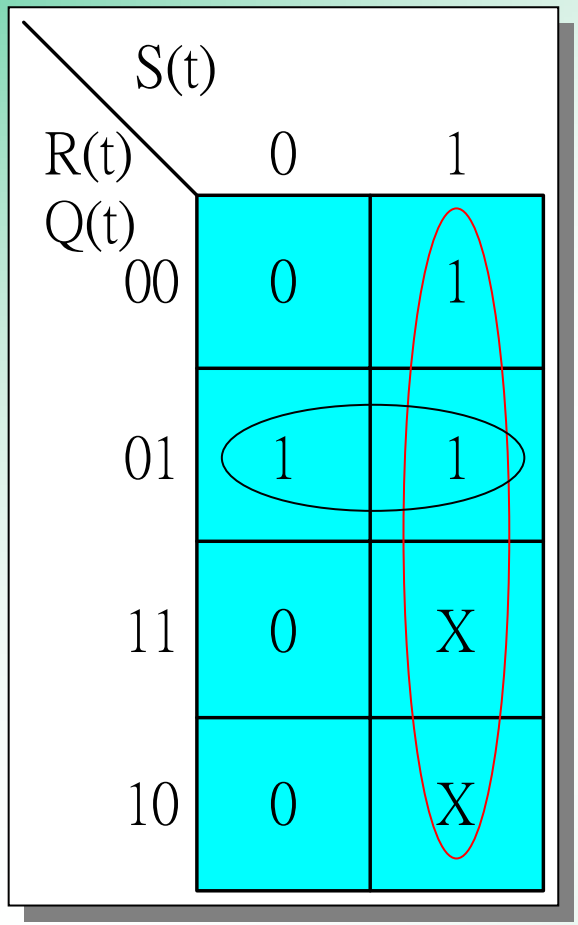
$Q_t^+(Q_{n+1})$: Next State

inputs not allowed



$$Q(t+\varepsilon) = S(t) + R'(t)Q(t) \qquad (SR = 0) \text{ or}$$

$$\underbrace{Q^{+} = S + R'Q}_{\text{characteristic equation}} \qquad (SR = 0)$$

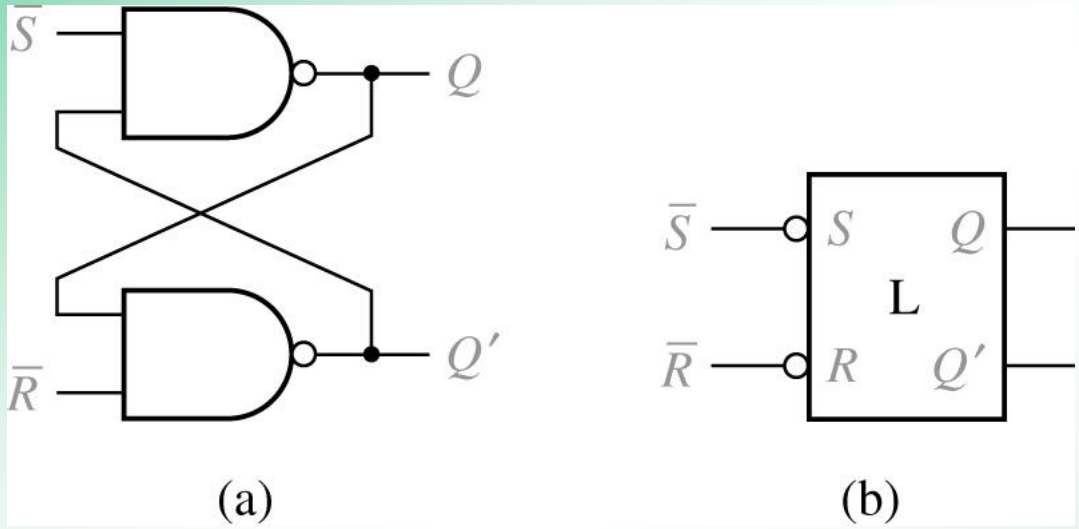


S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

Qn : present state

Qn + 1 : next state

Alternative form using NAND gates



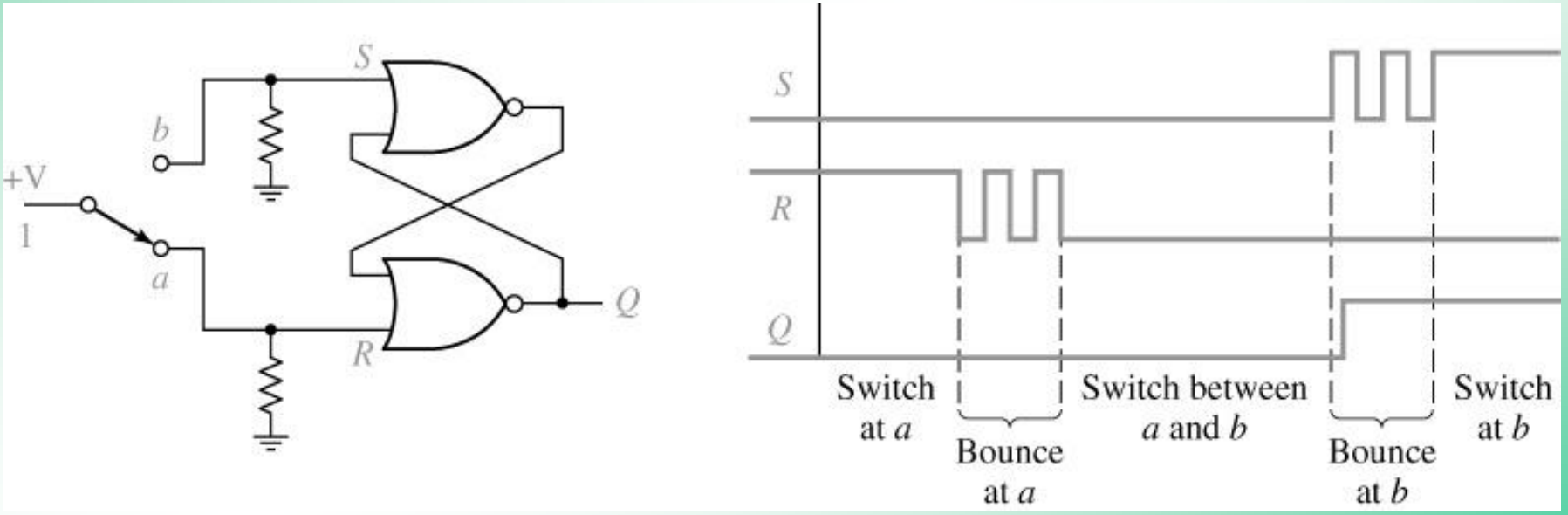
$\overline{S}$	$\overline{R}$	Q_{n+1}
1	1	Q_n
1	0	0
0	1	1
0	0	–

Qn : present state

Qn + 1 : next state

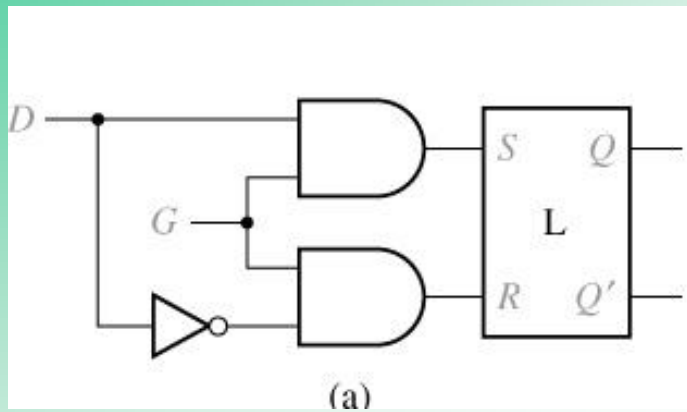
Usage of SR latch

1. As component in more complex latches and FFs
2. For debouncing switches

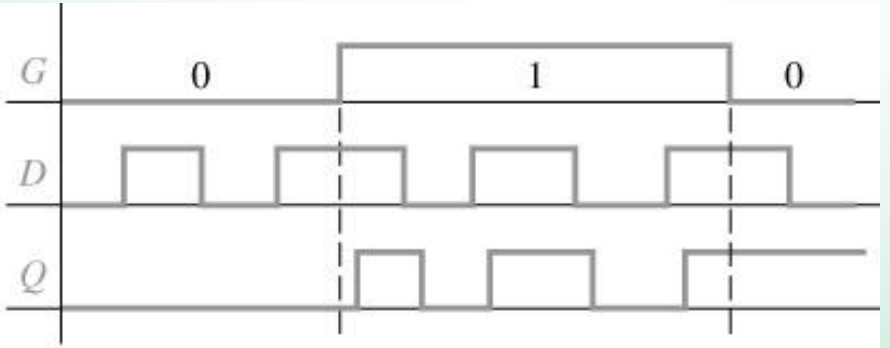


Gated D Latch

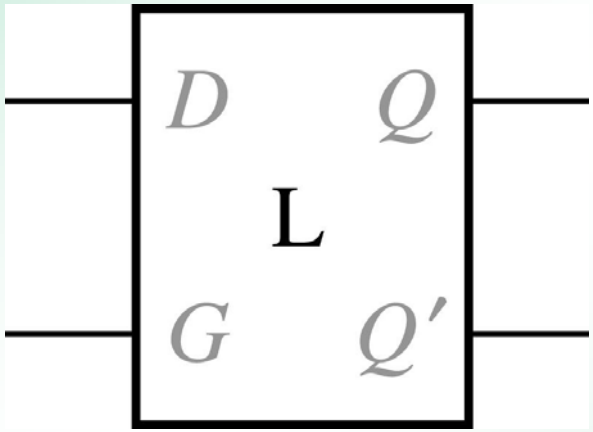
Transparent latch since G=1, Q = D

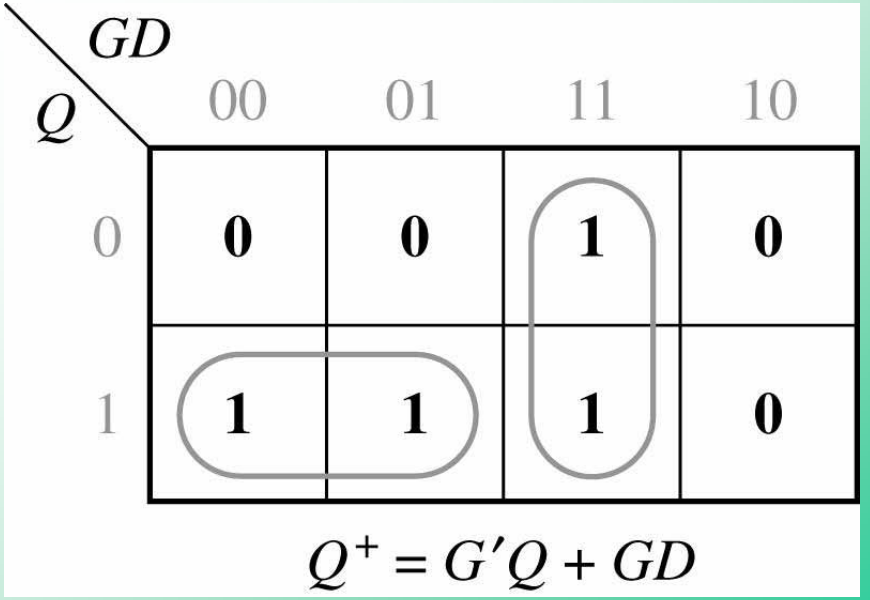


(a)



(b)

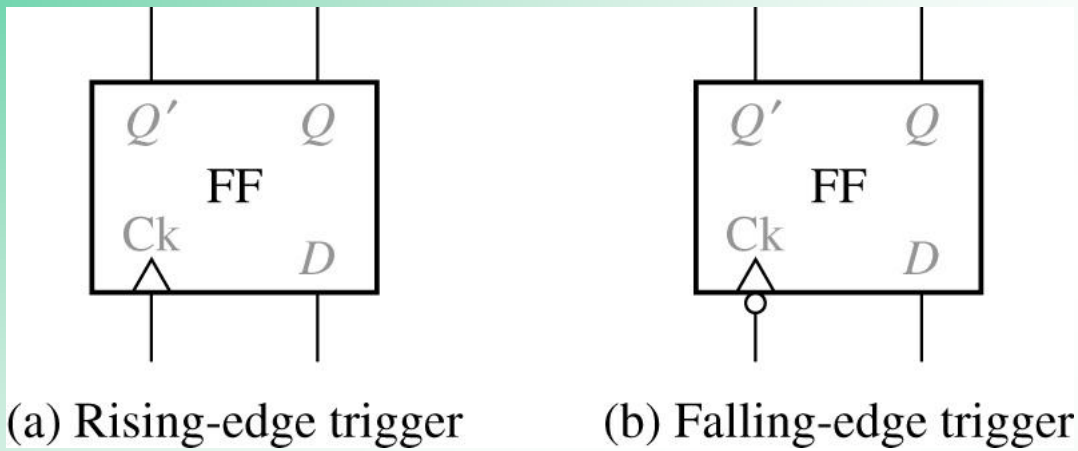




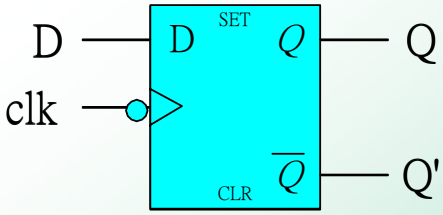
$Q^+ = G'Q + GD$

Edge-Triggered D Flip-Flop

Similar to D latch, but changes only to clock edge



(a) Rising-edge trigger (b) Falling-edge trigger

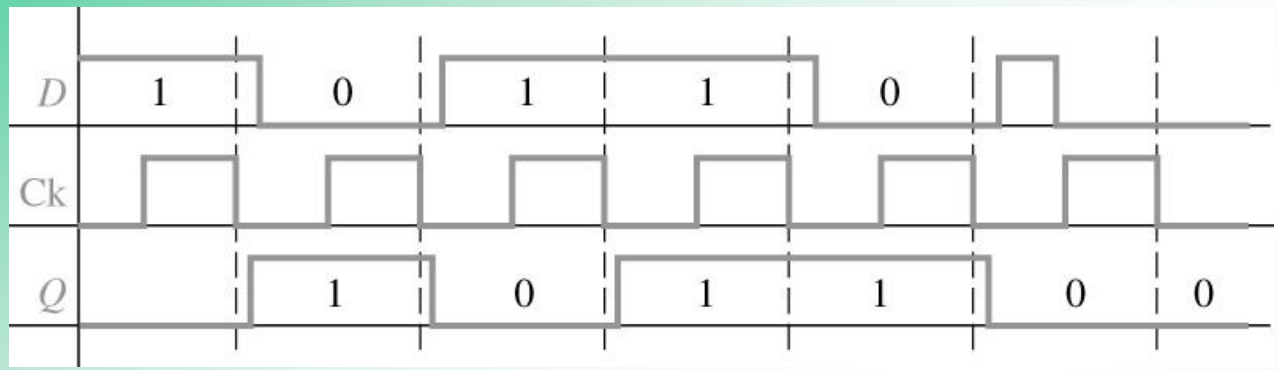


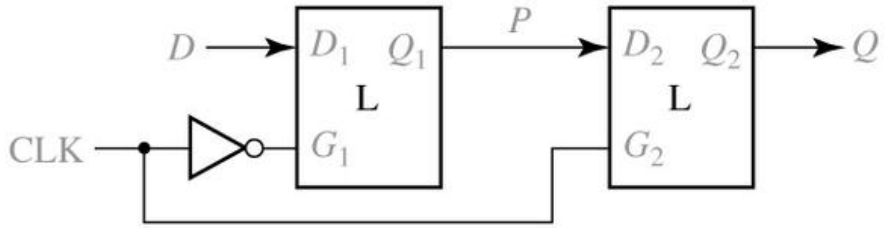
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

D	Q_n^+
0	0
1	1

$Q^+ = D$

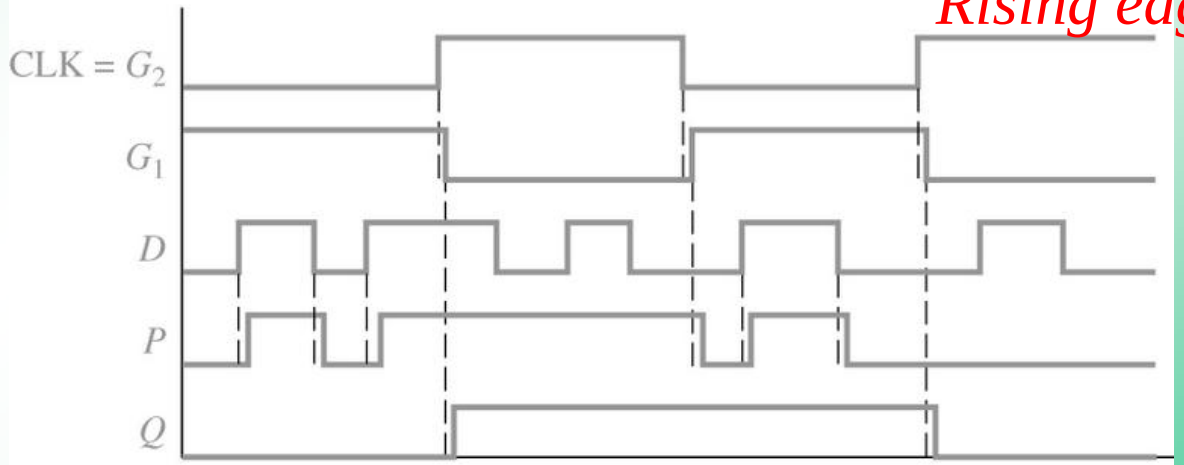
Timing diagram of falling edge triggered DFF





(a) Construction from two gated D latches

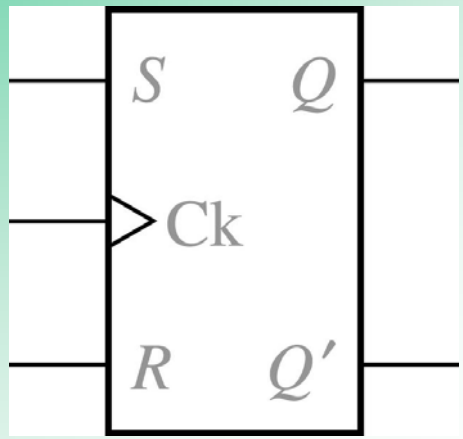
Rising edge



(b) Time analysis

SR Flip-Flop

Similar to SR latch, but changes only to clock edge, and extra clock in

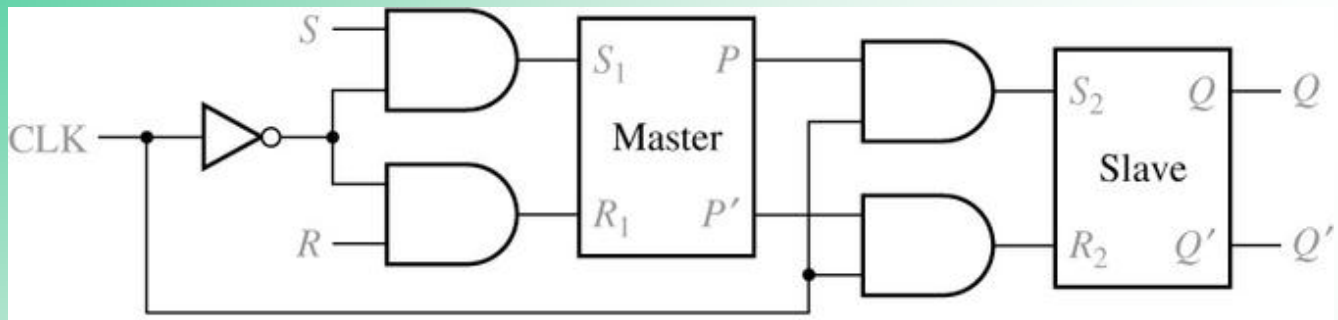


S	R	Q_{n+1}
0	0	Q_n (no state change)
0	1	0(reset Q to 0, after active CLK edge)
1	0	1(set Q to 1, after active CLK edge)
1	1	– (not allowed)

Qn : present state

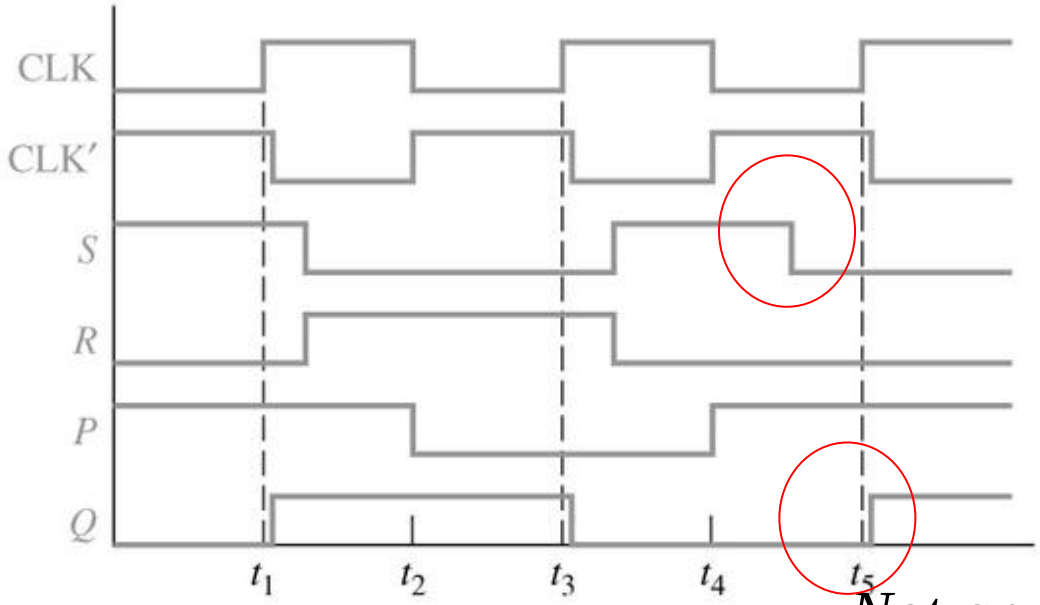
Qn + 1 : next state

SR implementation and timing



(a) Implementation with two latches

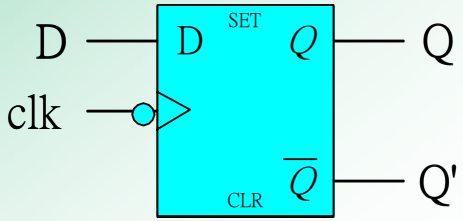
Master-slave FF

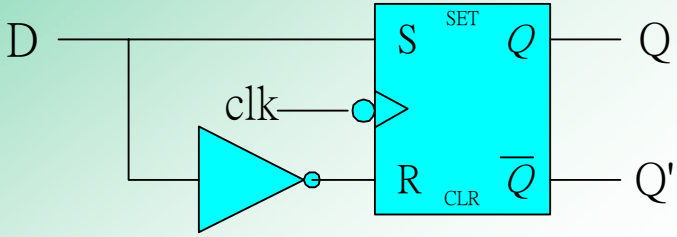


(b) Timing analysis

Not an edge-triggered FF

D F/F (Delay F/F)

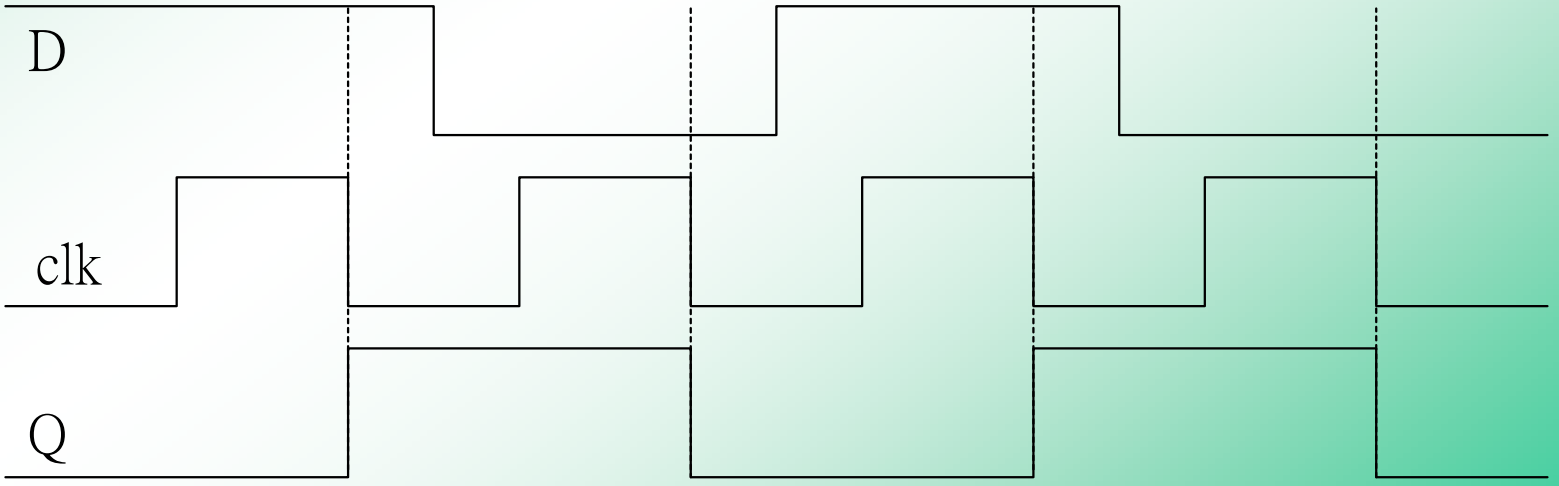




D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

D	Q_n^+
0	0
1	1

$Q^+ = D$



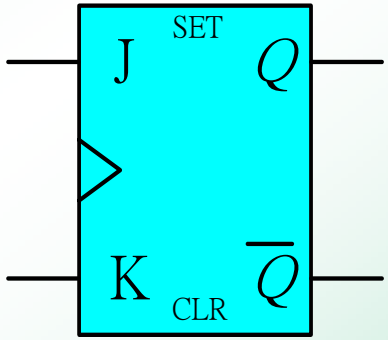
J-K F/F

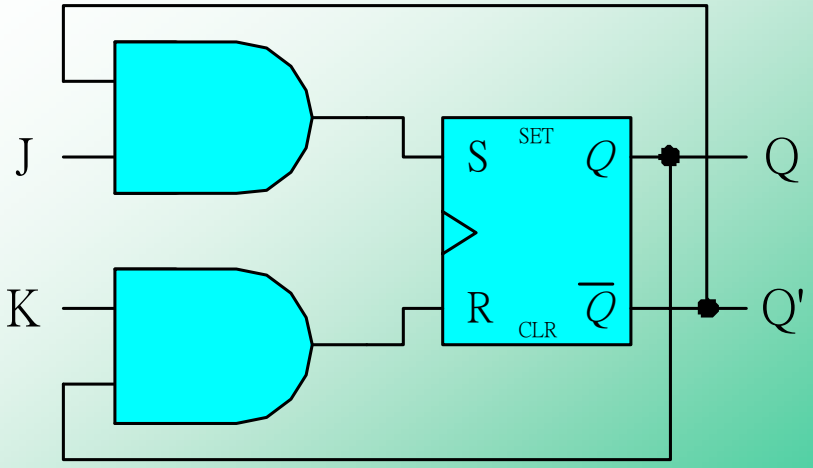
Extended version of SR FF

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q^+ = QK' + Q'J$$

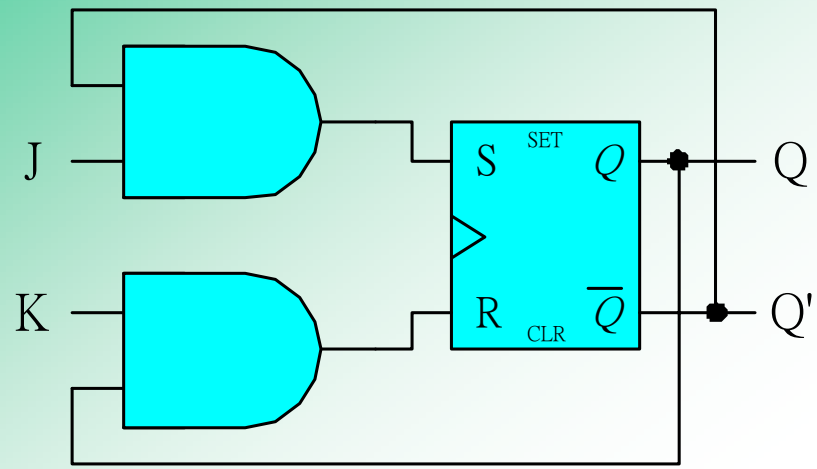
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$





$J = K = 1:$ $J-K$ F/F acts as a T-F/F

otherwise : J-K F/F acts as a S-R F/F



$$\begin{cases} J=1, K=0 \Rightarrow Q^{+}=1 \\ J=0, K=1 \Rightarrow Q^{+}=0 \\ J=0, K=0 \Rightarrow Q^{+}=Q \\ J=1, K=1 \Rightarrow Q^{+}=Q' \end{cases}$$

Timing Problem :

If $J = K = 1$, do not arrive at the same time

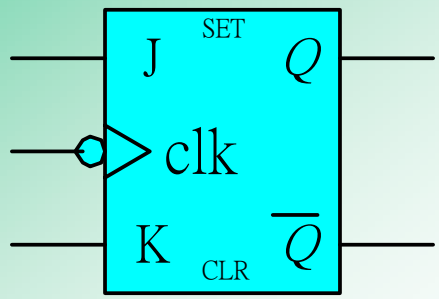
$\Rightarrow$ may $J = 0, K = 1$

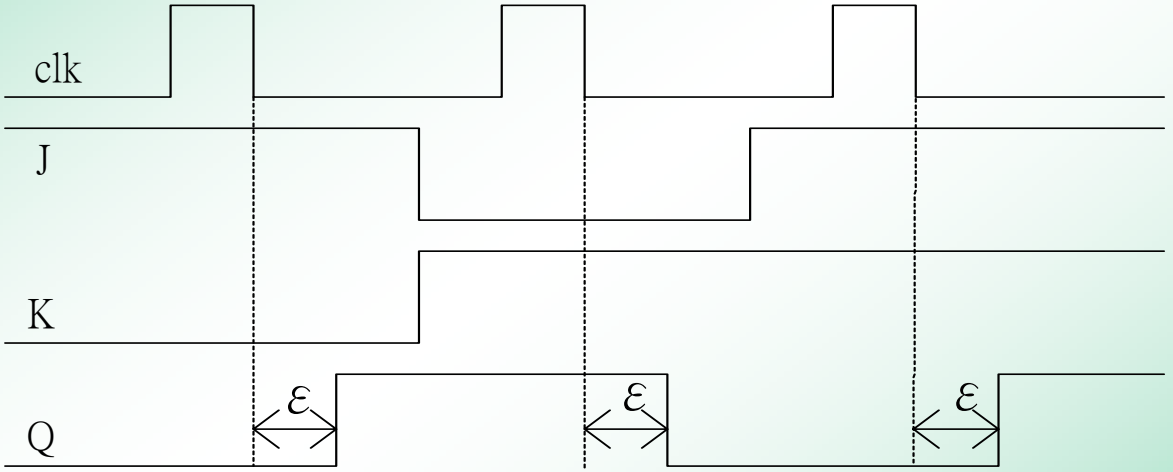
or too long

$\Rightarrow$ Q may $0 \rightarrow 1 \rightarrow 0 \rightarrow 1$ oscillation

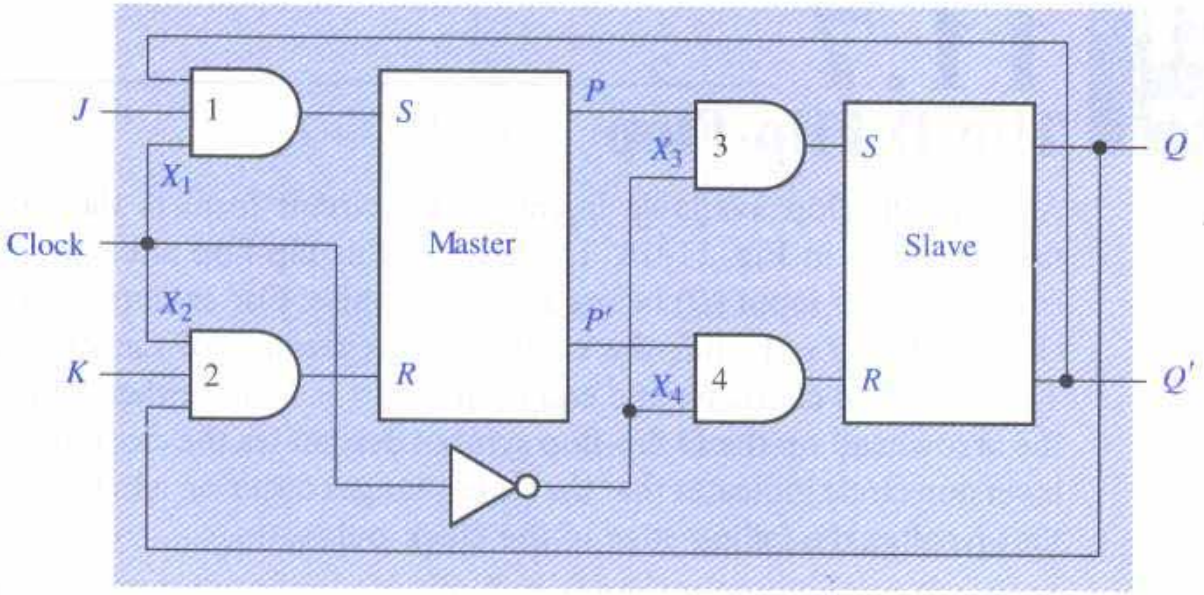
$\Rightarrow$ Using clocked J-K F/F

Clocked JK F/F

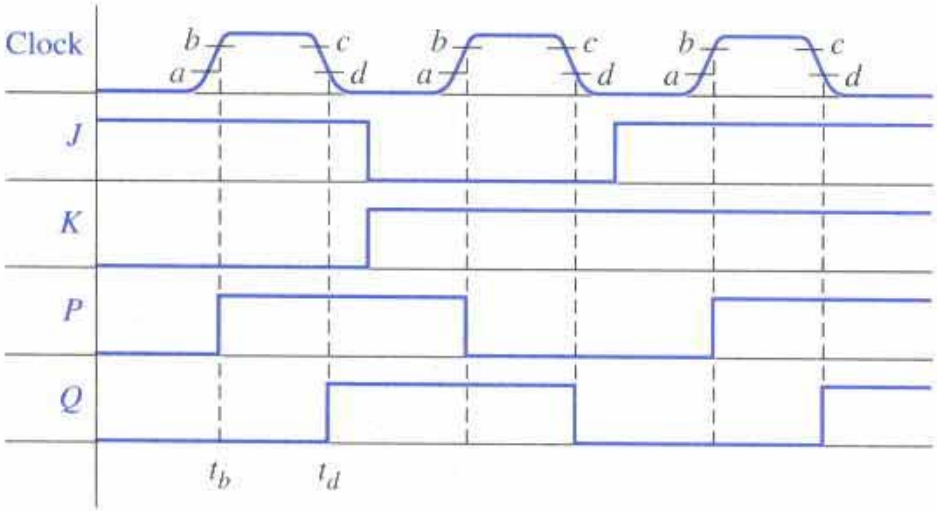




The Change of F/F state always occurs on the **falling edge** of the CLK pulse regardless **pulse width**



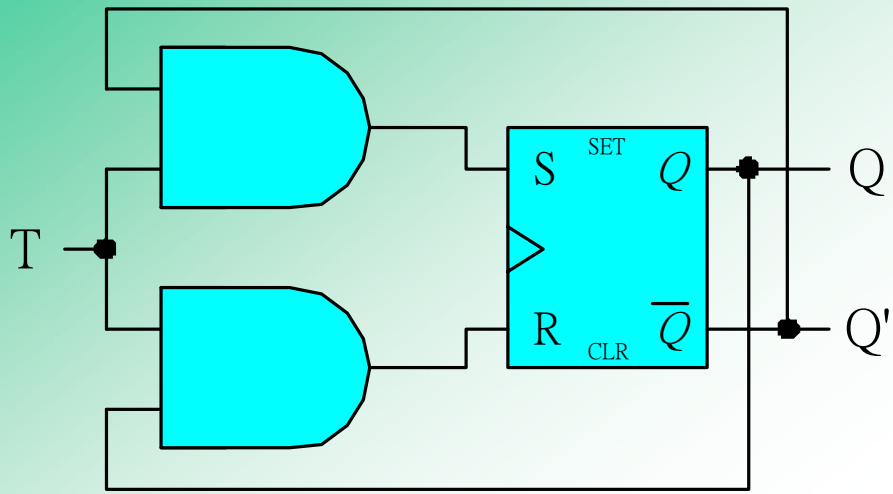
(a) Master-slave J-K flip-flop

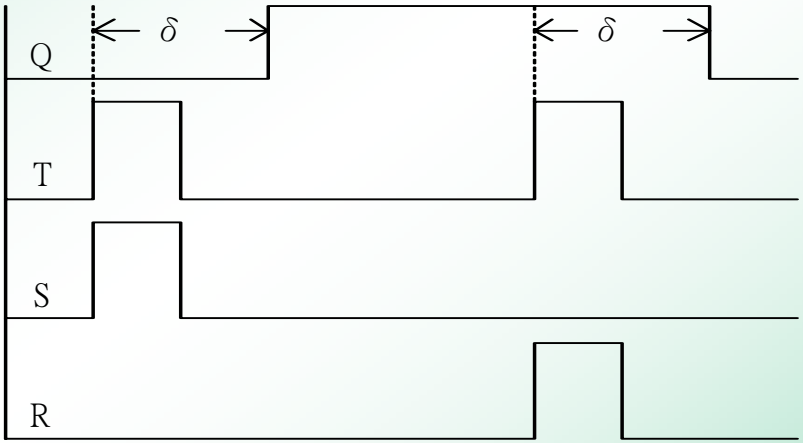


(b) Internal timing diagram for master-slave J-K flip-flop

Trigger F/F (T-F/F)

$$\begin{cases} R = QT \\ S = Q'T \end{cases} \quad i.e \quad Q = 1 \xrightarrow{\text{next input}} R = 1 \qquad \xrightarrow{\text{next state}} Q = 0$$



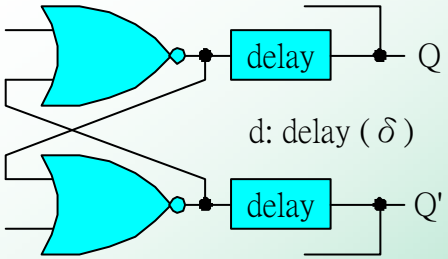


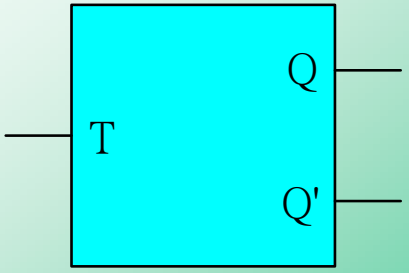
T	Q	Q_n^+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_n^+ = T'Q + TQ'$$

$$= T \oplus Q$$

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$





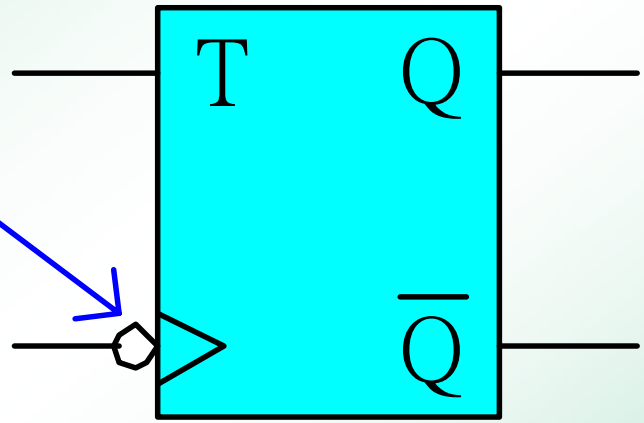
δ : 1AND + 2NOR gate delay

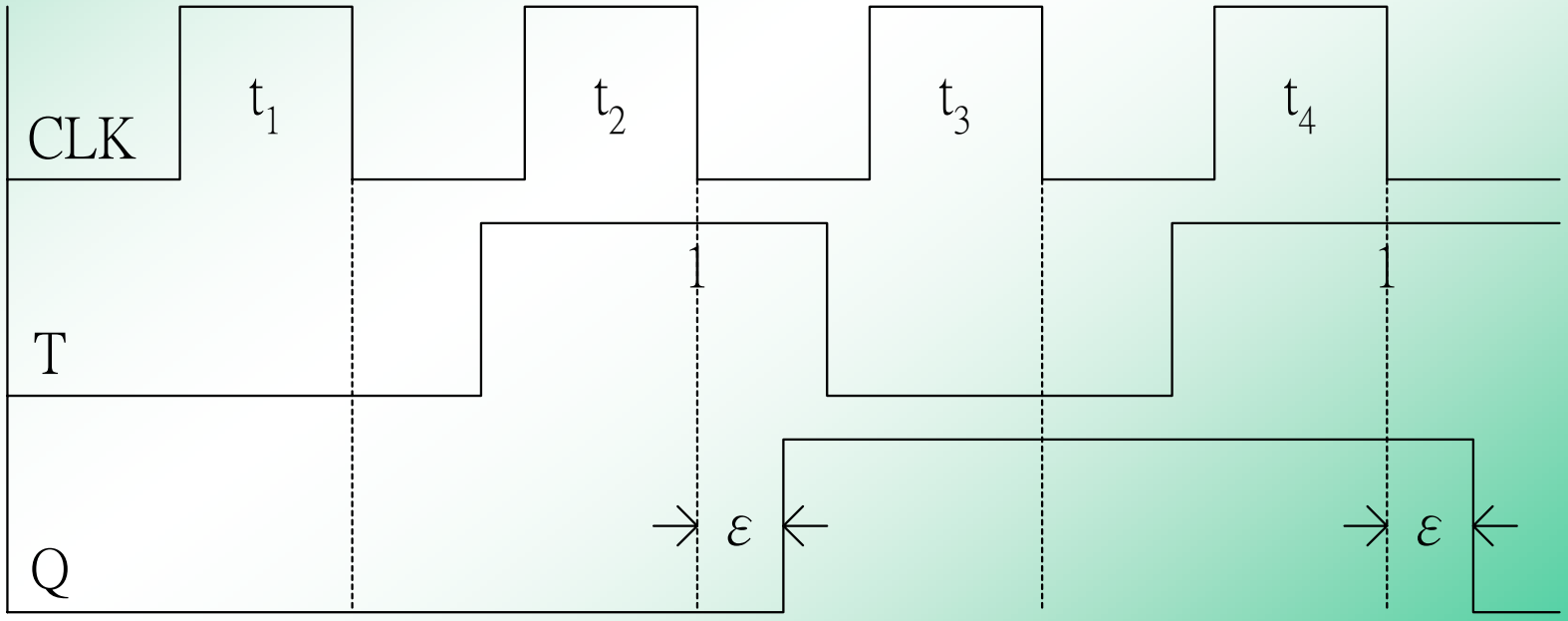
T must terminate before Q changes state

so we add a delay.

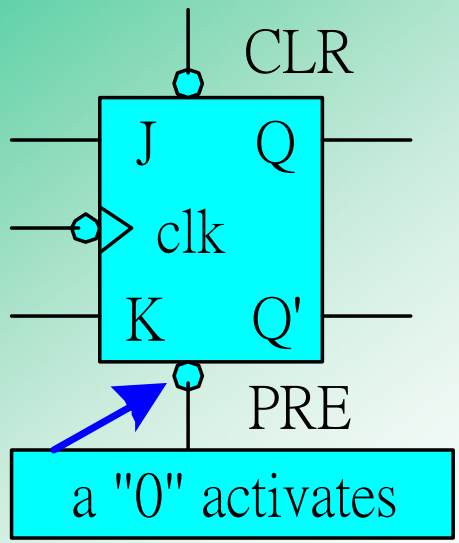
Clocked T F-F: For Synchronous design

falling edge triggering.
(Negative edge triggering)





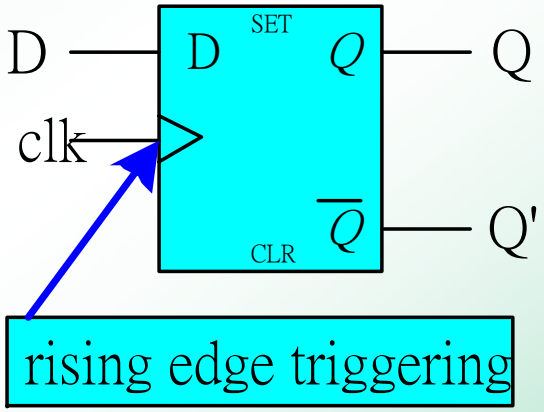
Clocked F/F with Clear and Preset

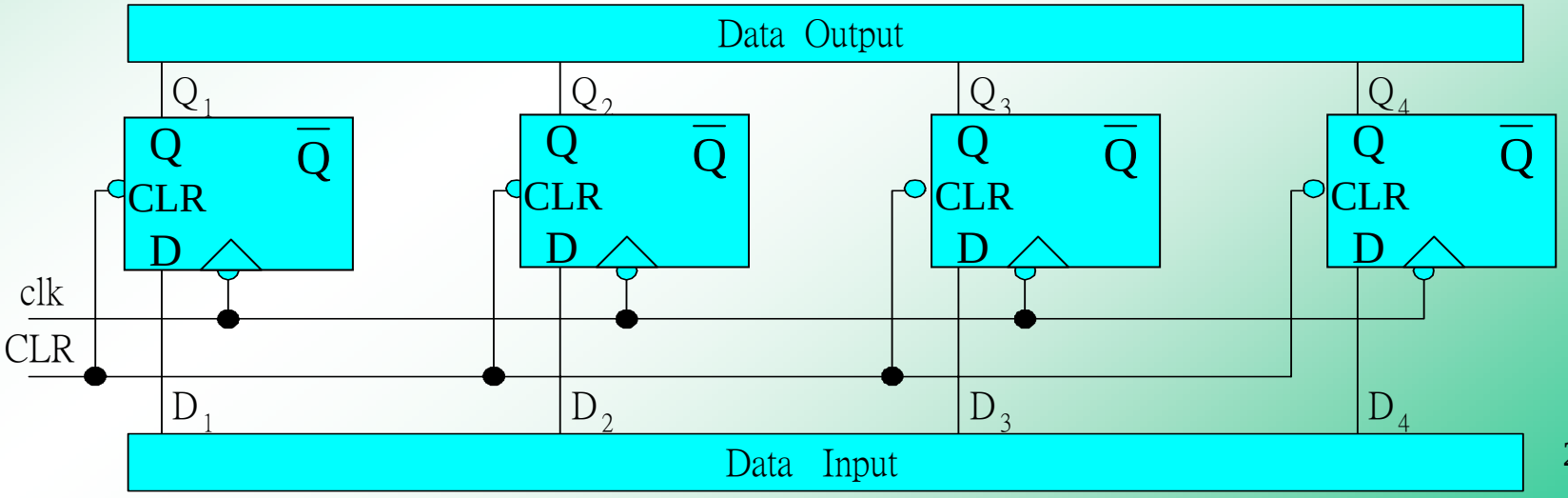


$$CLR = 0 \Rightarrow Q = 0$$

$$PRE = 0 \Rightarrow Q = 1$$

$$CLK = PRE = 1 \Rightarrow \textit{Normal Opeartion}$$

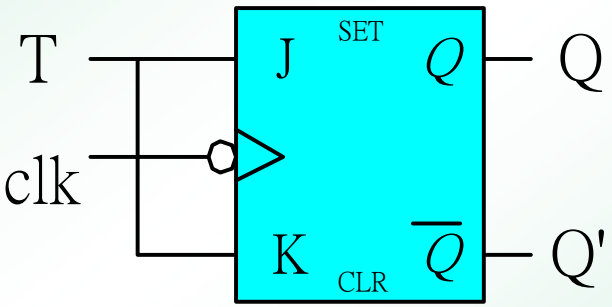


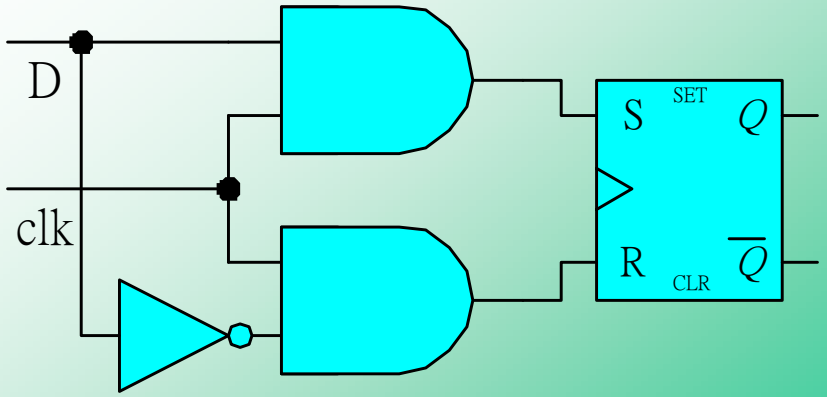


Characteristic Equations

$Q^+ = S + R'Q$	SR F / F	$(SR = 0)$ SR 不同時爲 1
$Q^+ = T \oplus Q$	T F / F	
$Q^+ = JQ' + K'Q$	JK F / F	
$Q^+ = D$	D F / F	

Conversion between F/F





HOMEWORK -- Unit 11

- 11.3
- 11.6
- 11.8
- 11.12
- 11.14
- 11.21