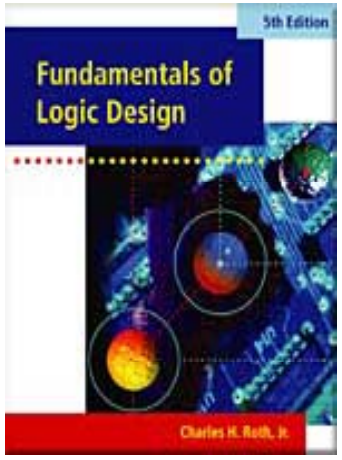
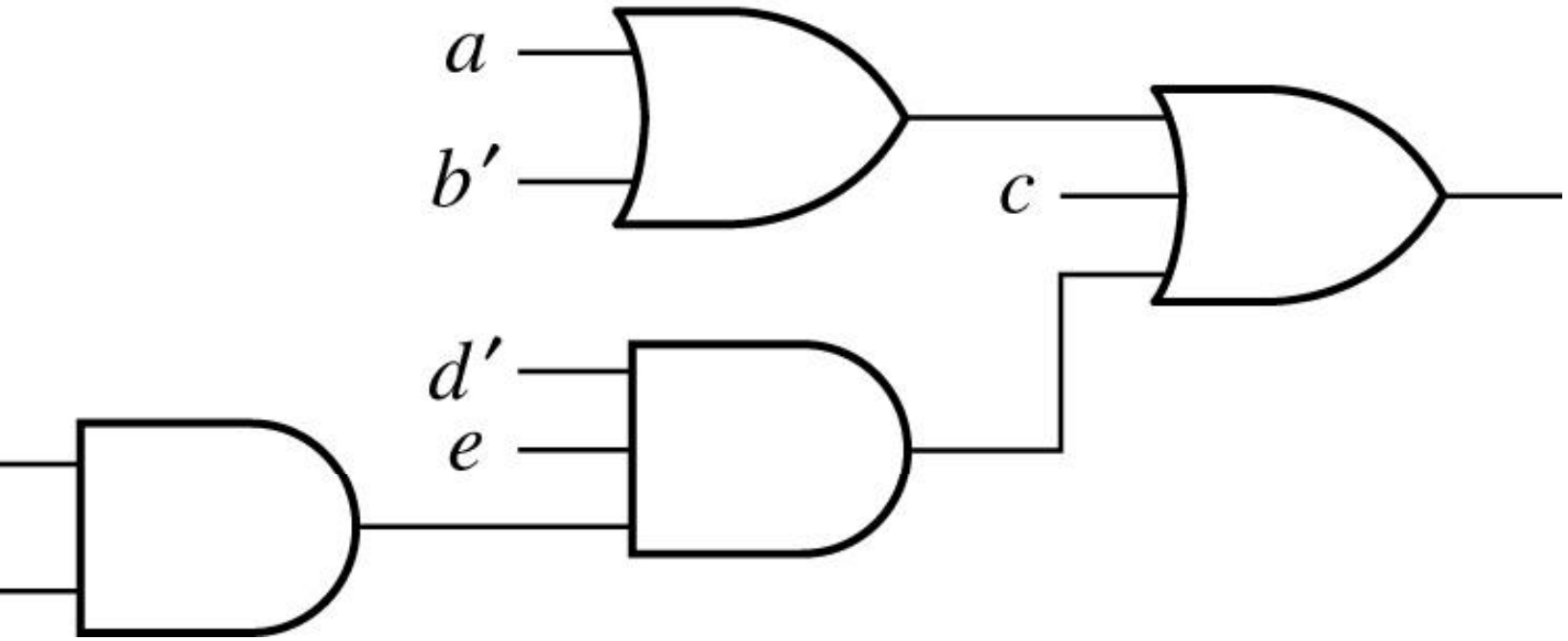
FIGURES FOR

CHAPTER 8

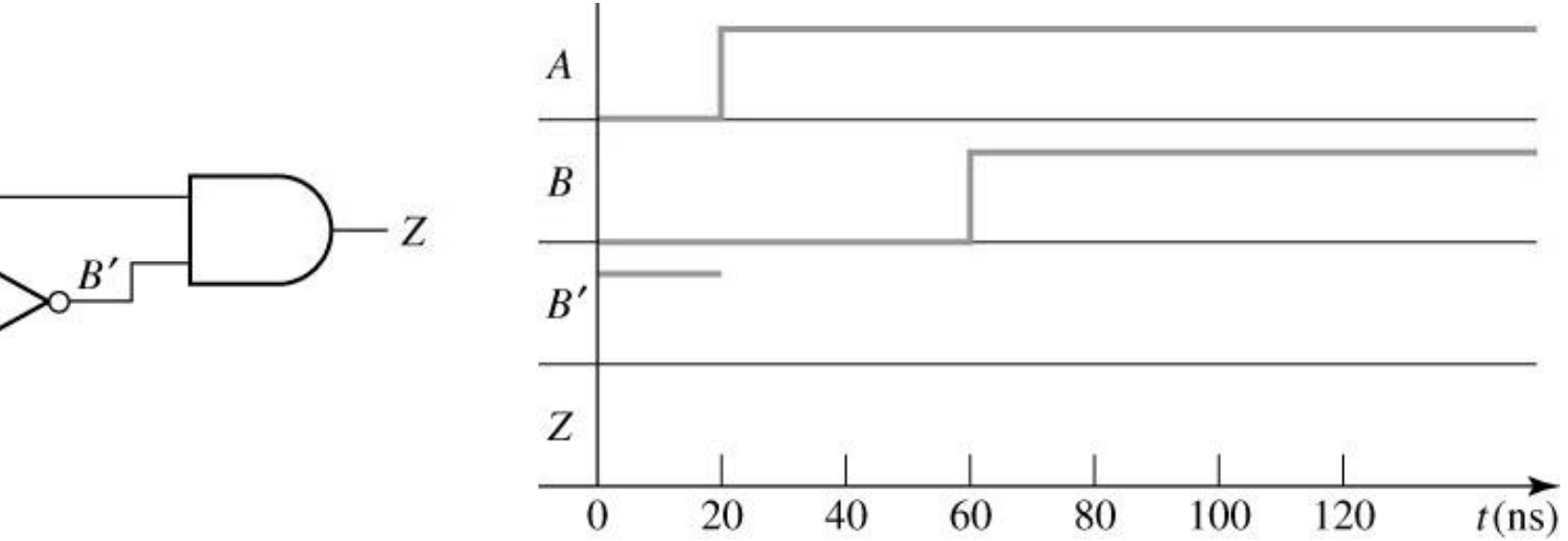
COMBINATIONAL CIRCUIT DESIGN AND SIMULATION USING GATES



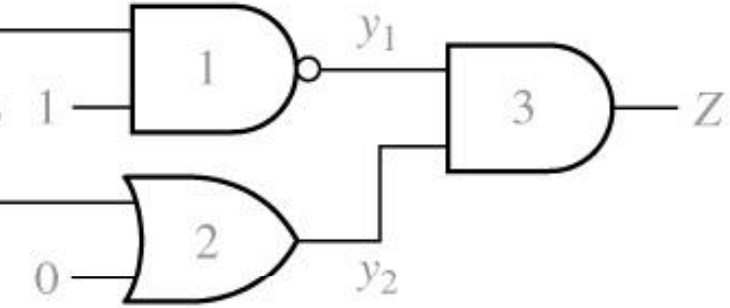
This chapter in the book includes:

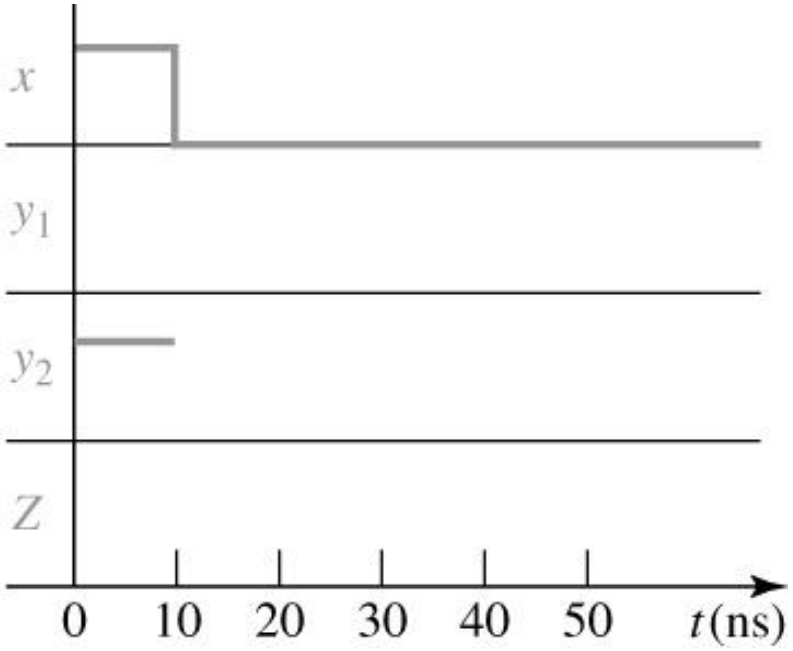


Study Guide, No. 3

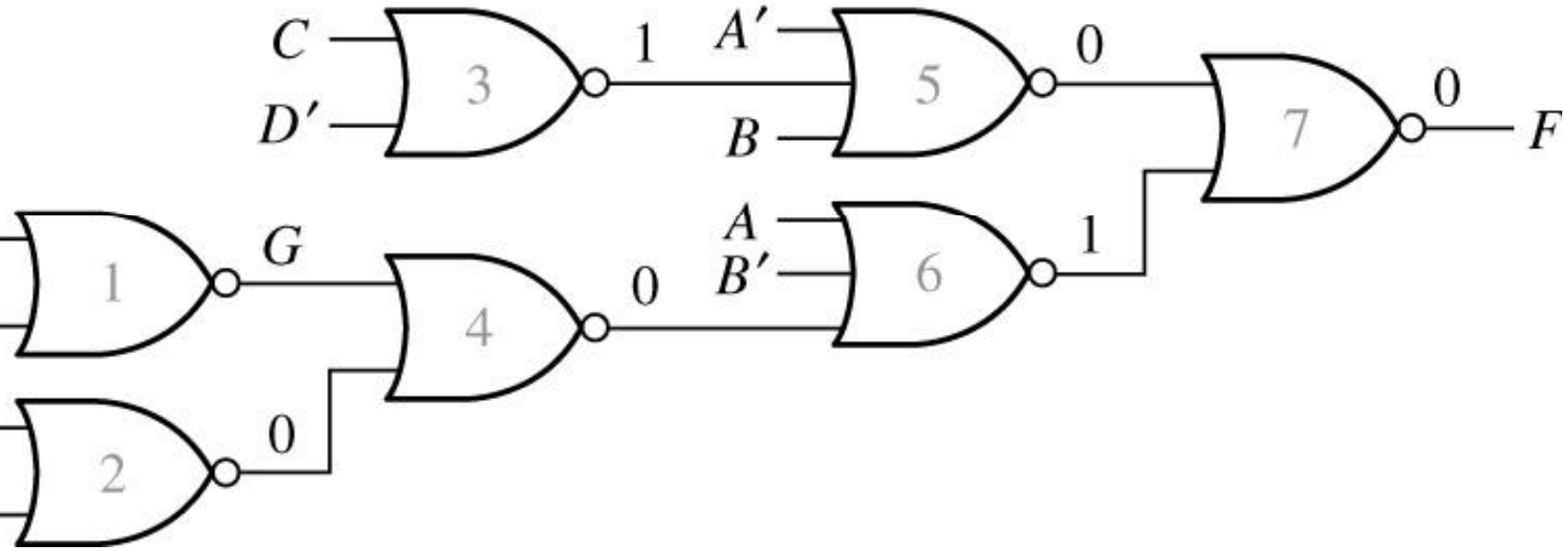


Study Guide, No. 5a



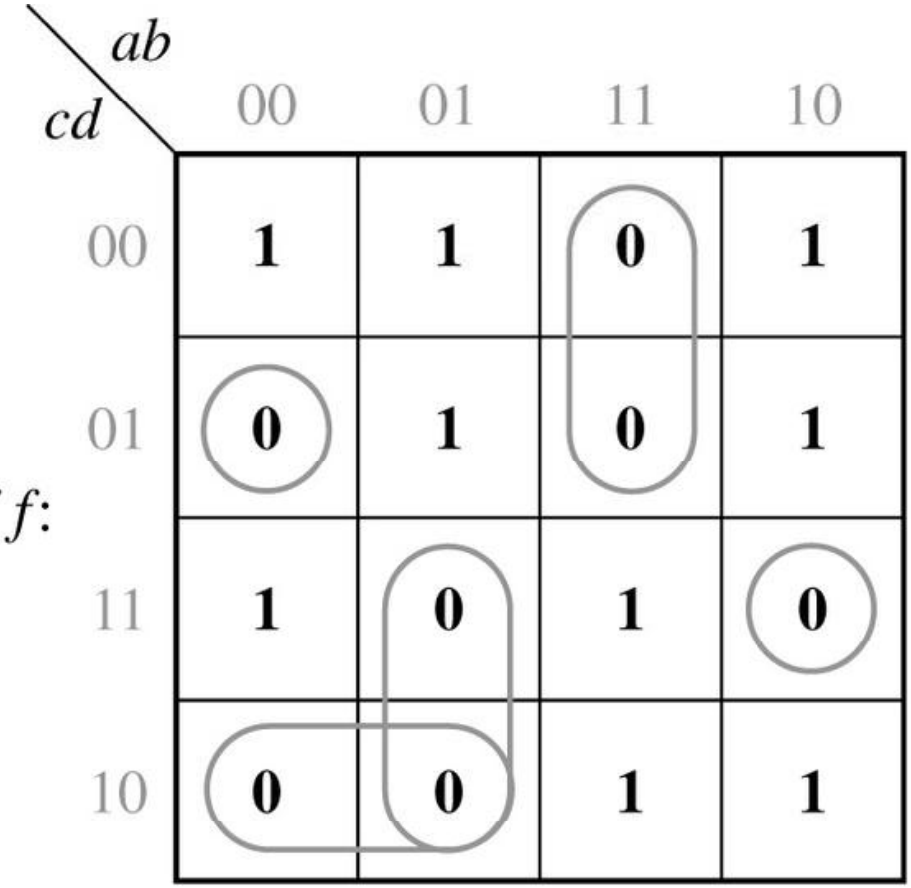


Study Guide, No. 6a



Study Guide, No. 7b

map of f:



$$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$$

Section 8.2, p. 206

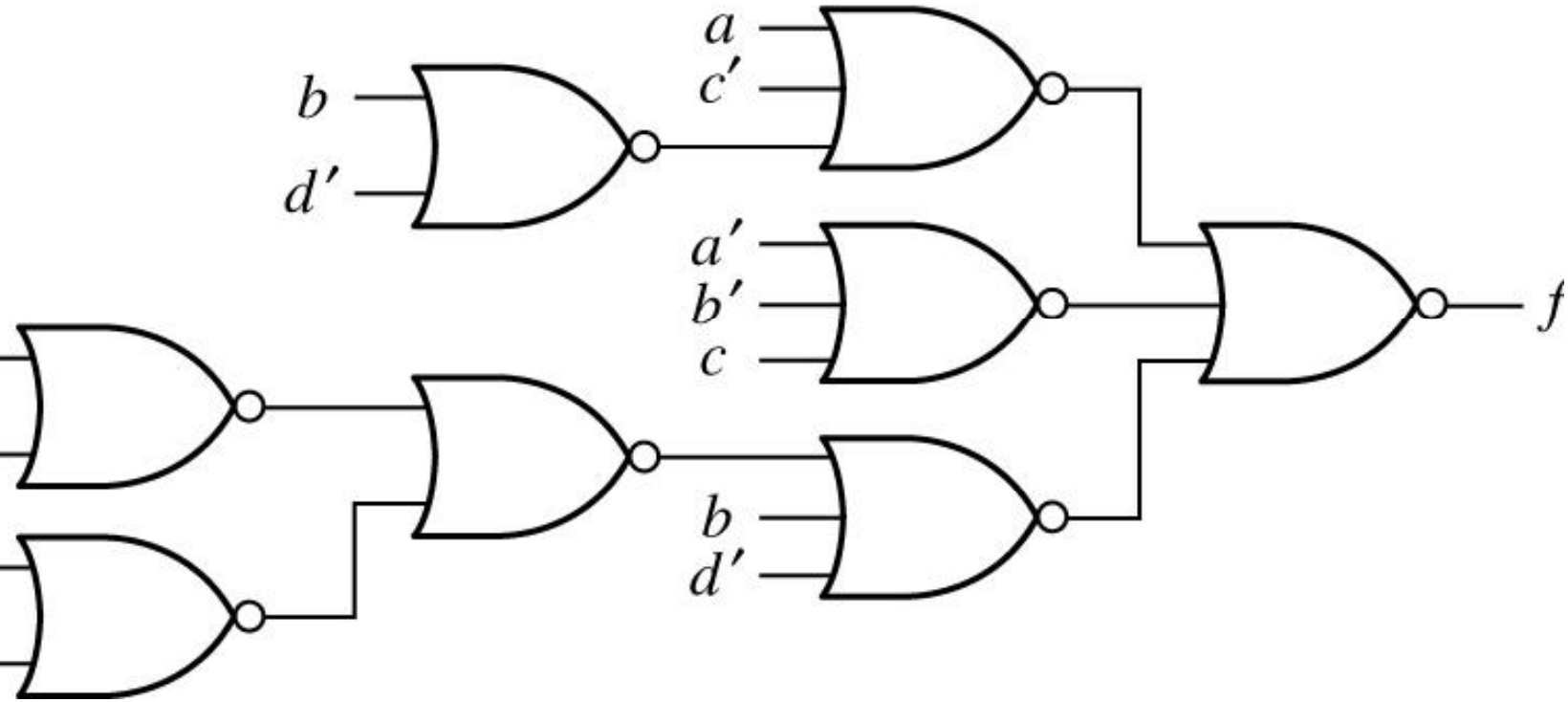
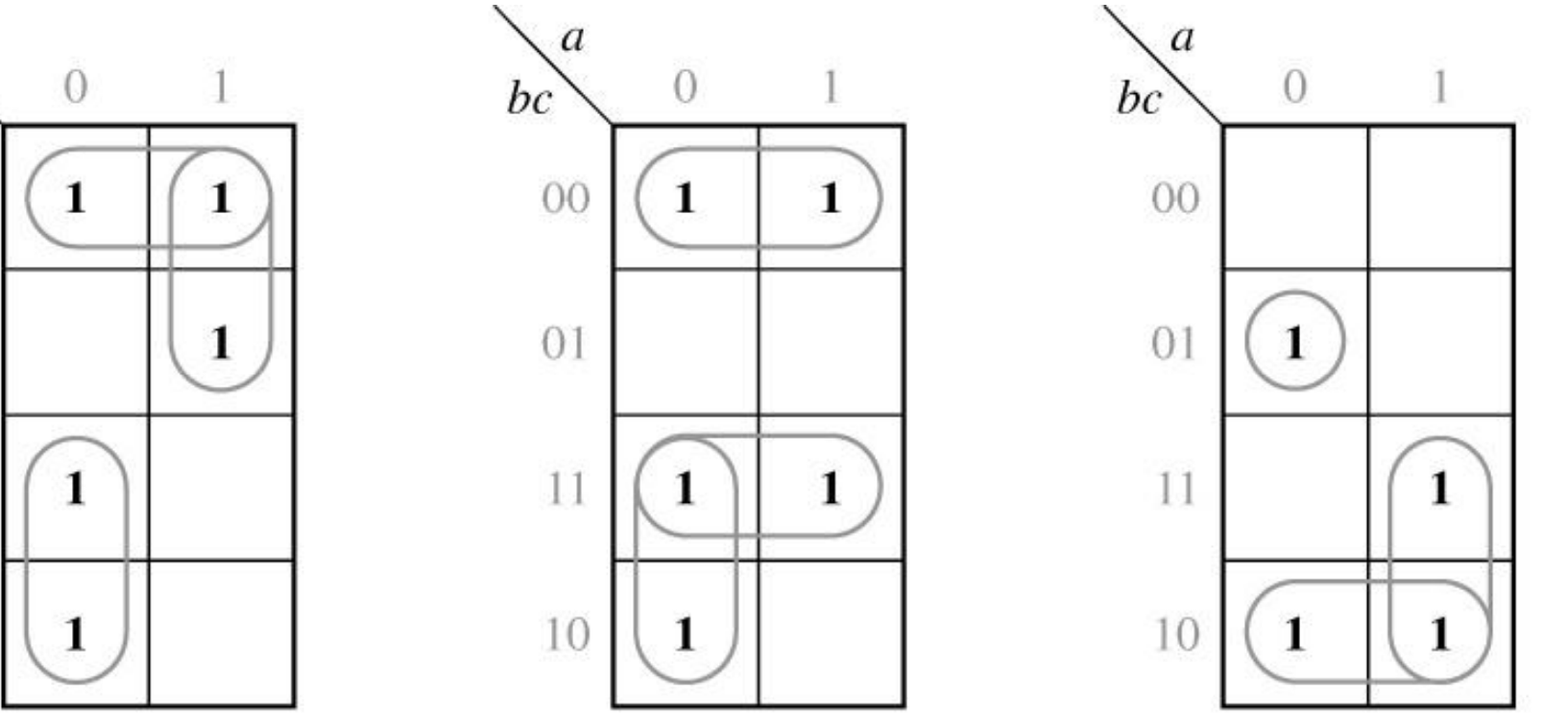


Figure 8-1



$= \Sigma m\,(0, 2, 3, 4, 5)$ $f_2 = \Sigma m\,(0, 2, 3, 4, 7)$ $f_3 = \Sigma m\,(1, 2, 6, 7)$

Figure 8-2

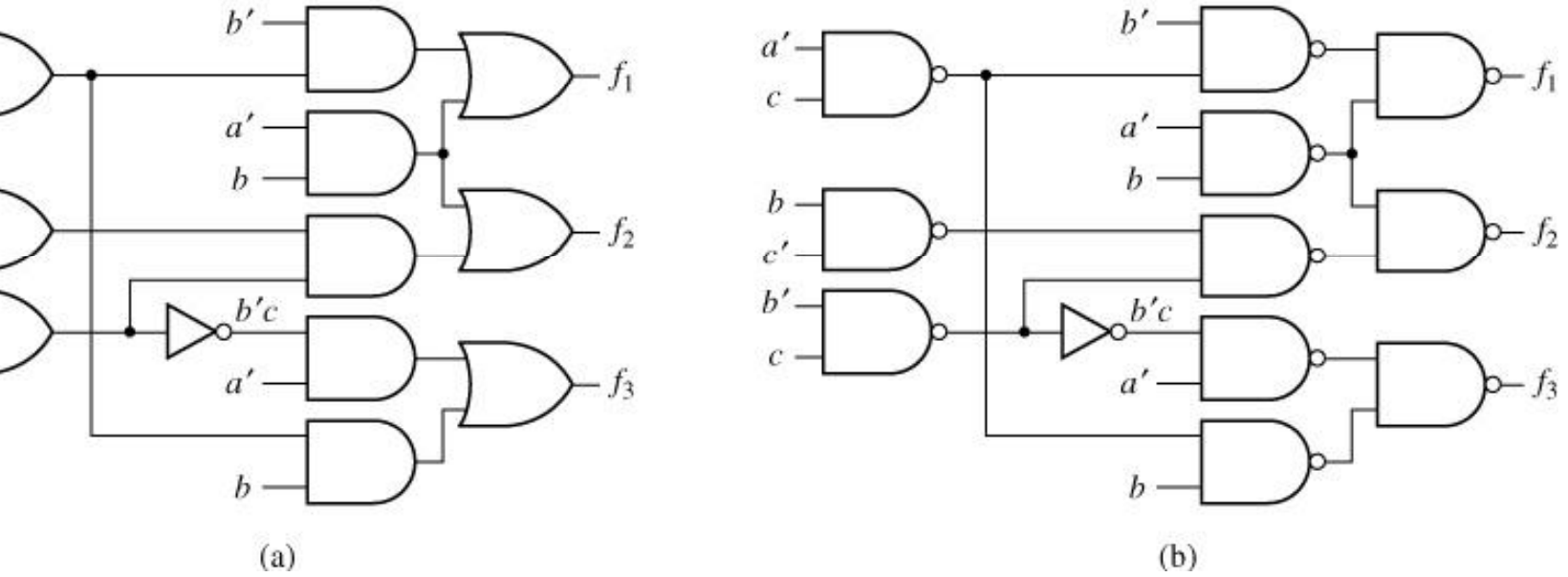


Figure 8-3: **Realization of Figure 8-2**

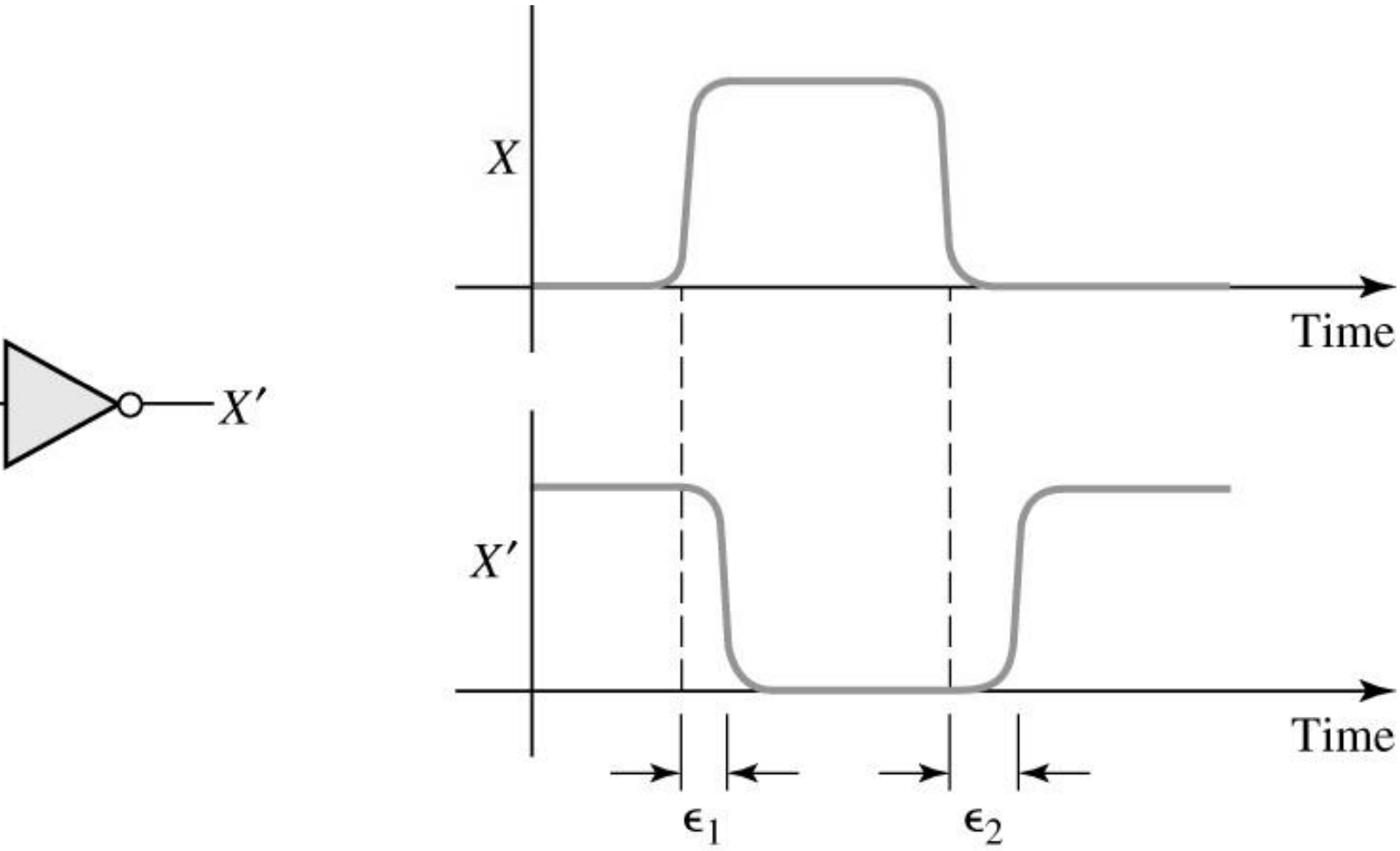
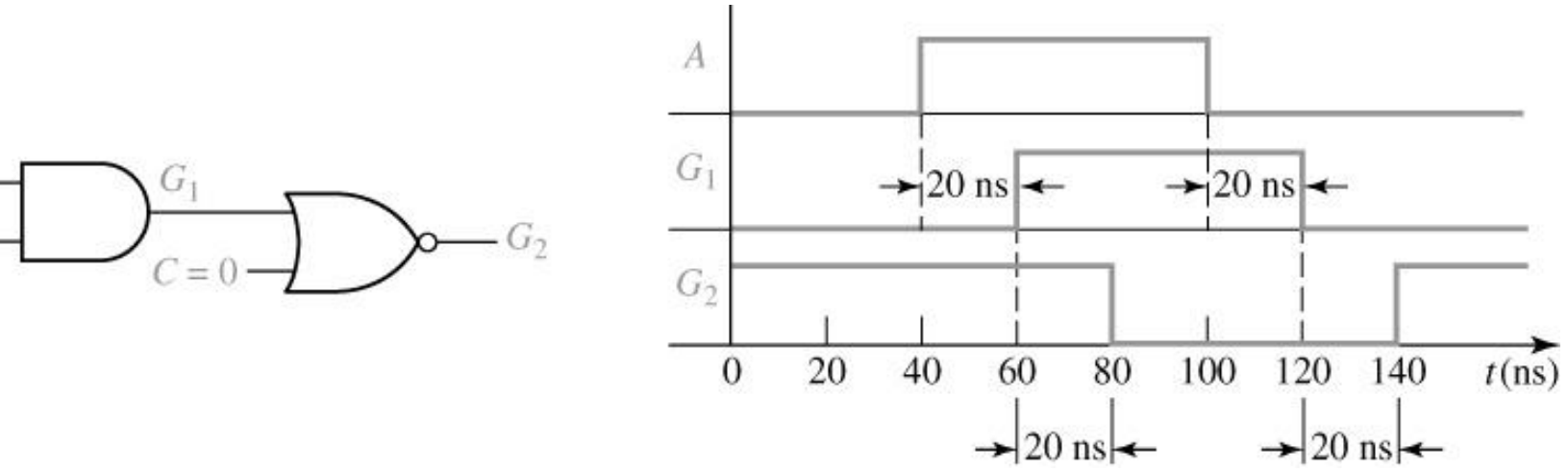
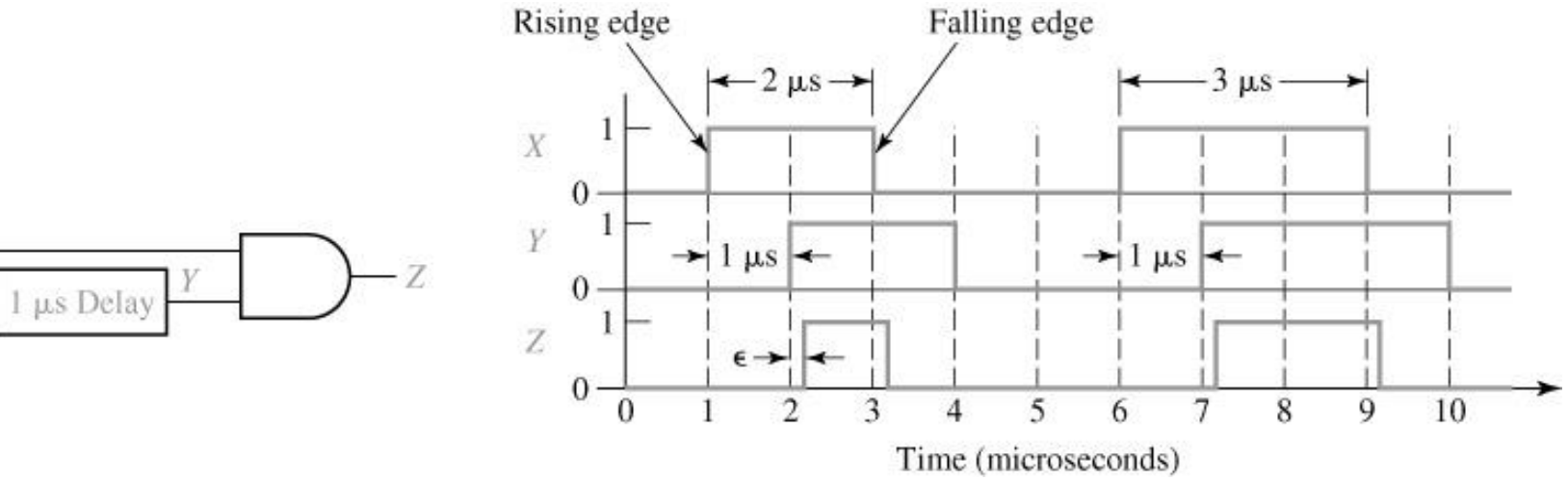


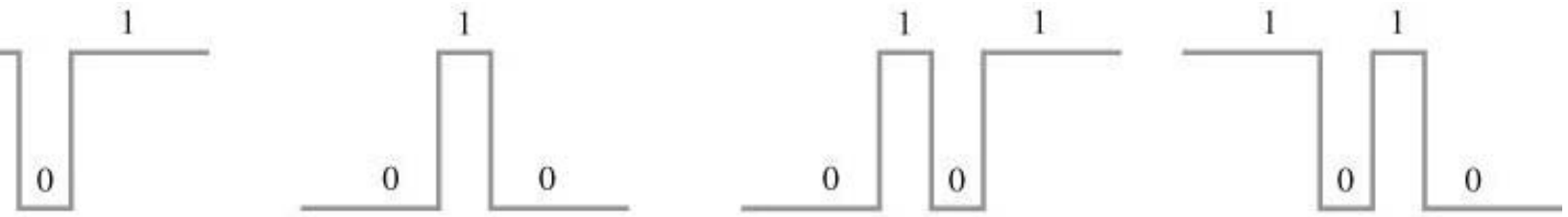
Figure 8-4: Propagation Delay in an Inverter



ure 8-5: **Timing Diagram for AND-NOR Circuit**

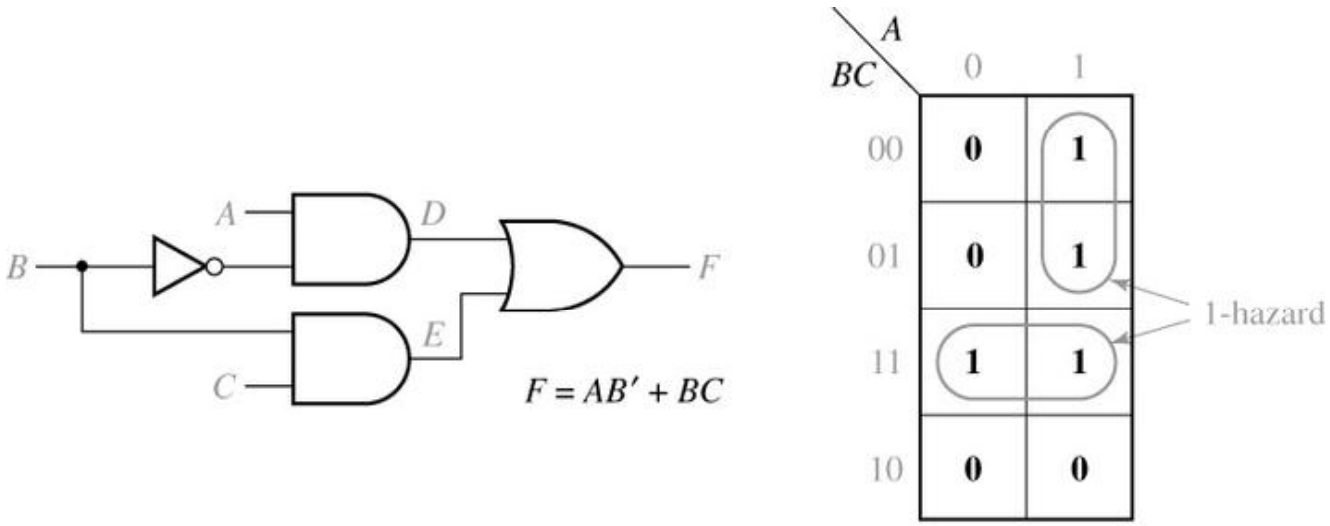


ure 8-6: Timing Diagram for Circuit with Delay

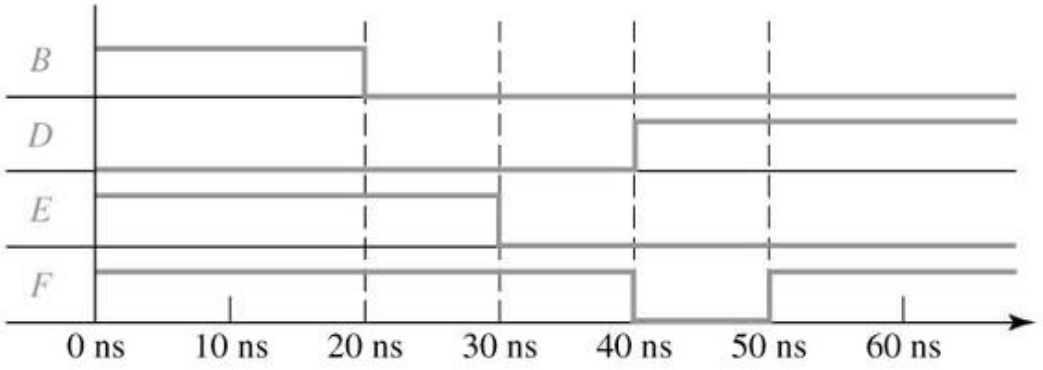


atic 1-hazard (b) Static 0-hazard (c) Dynamic hazards

Figure 8-7: **Types of Hazards**



(a) Circuit with a static 1-hazard



(b) Timing chart

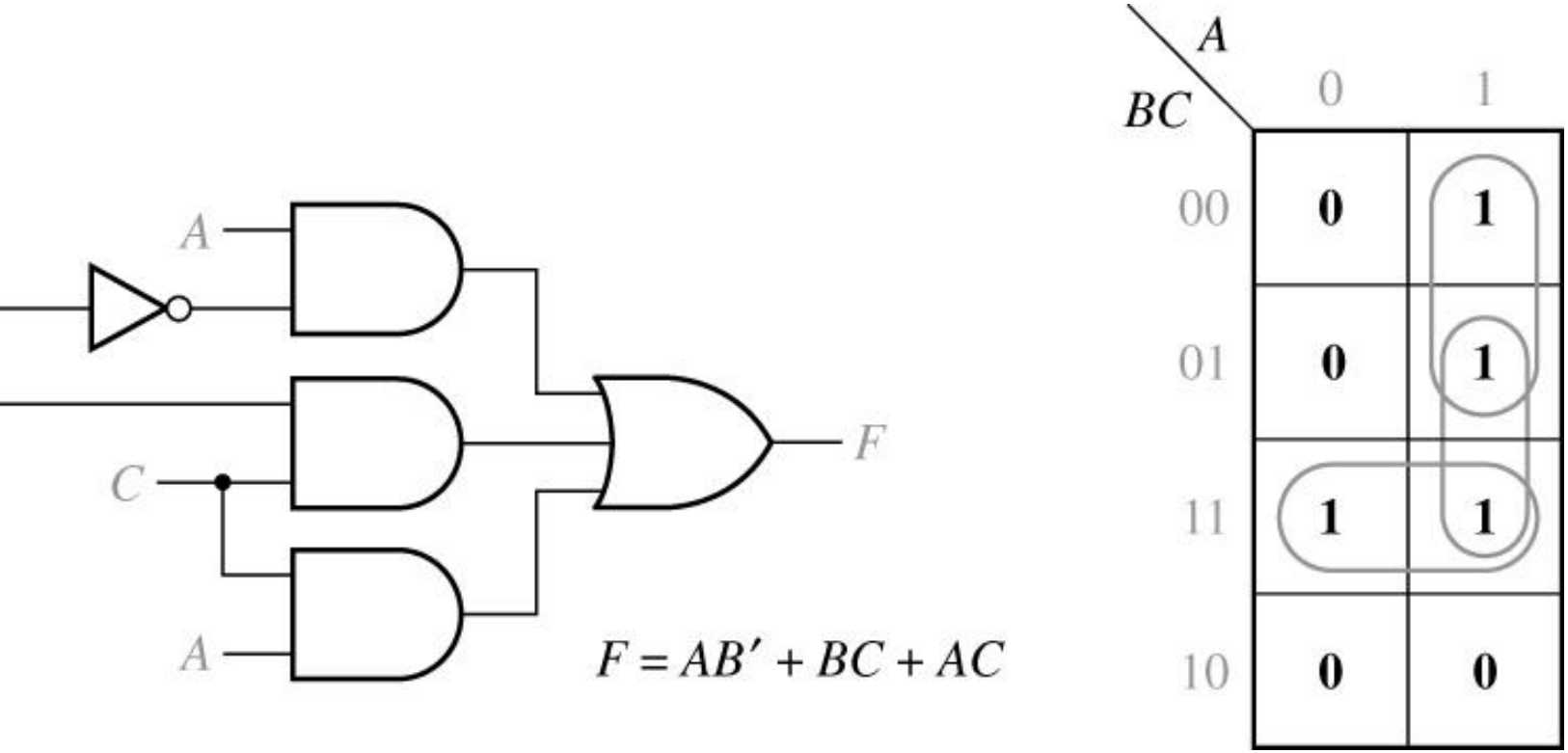
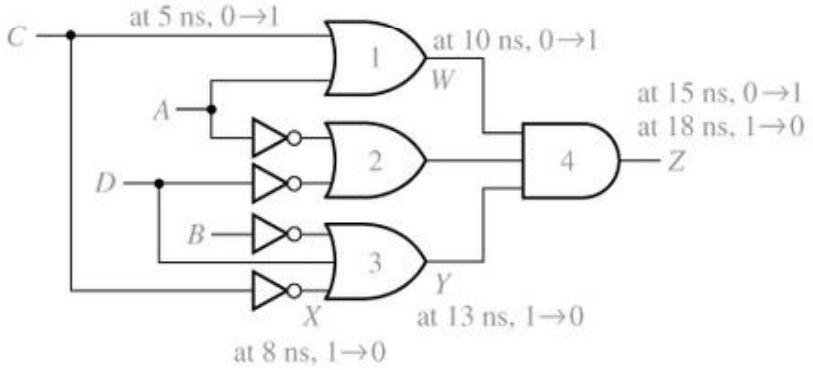
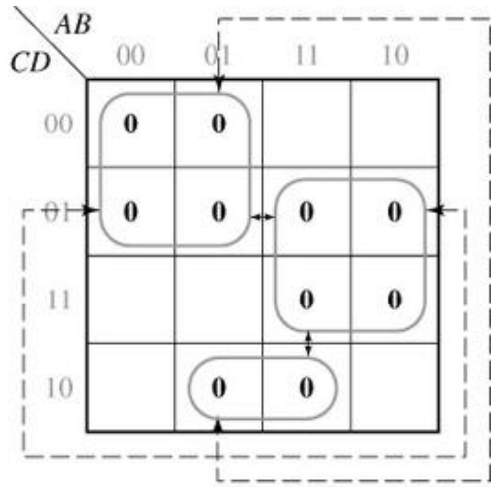


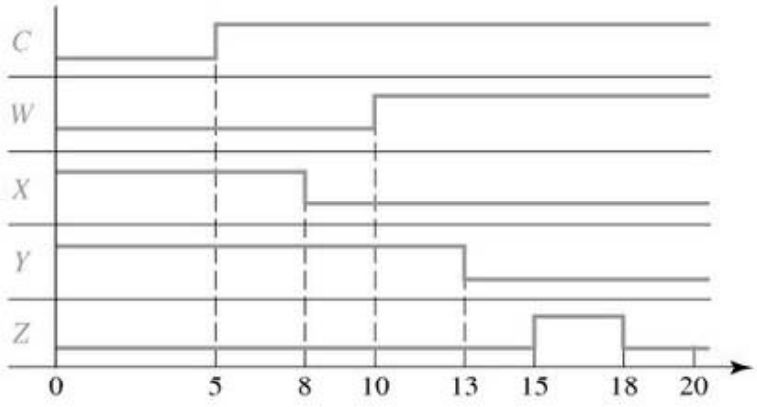
Figure 8-9: **Circuit with Hazard Removed**



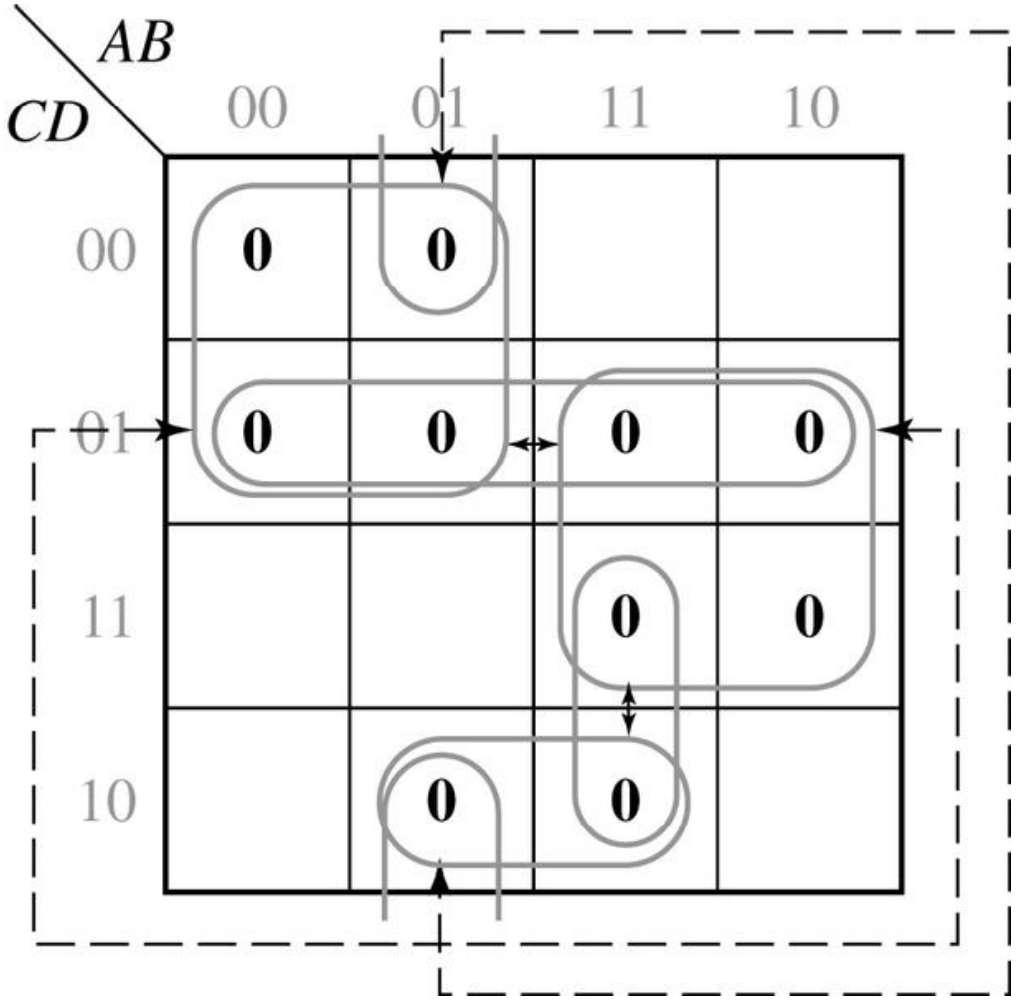
(a) Circuit with a static 0-hazard



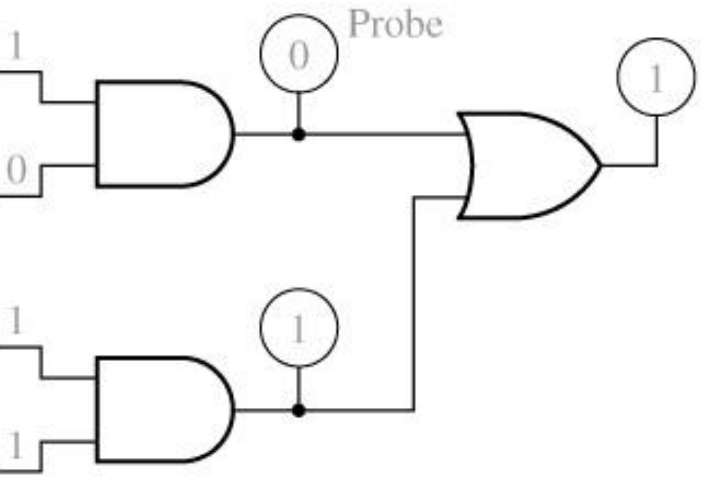
(b) Karnaugh map for circuit of (a)



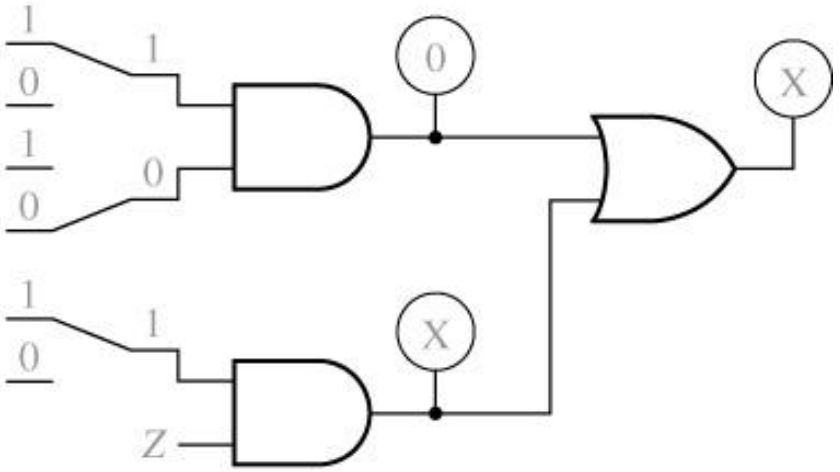
(c) Timing diagram illustrating 0-hazard of (a)



gure 8-11: Karnaugh Map Removing Hazards

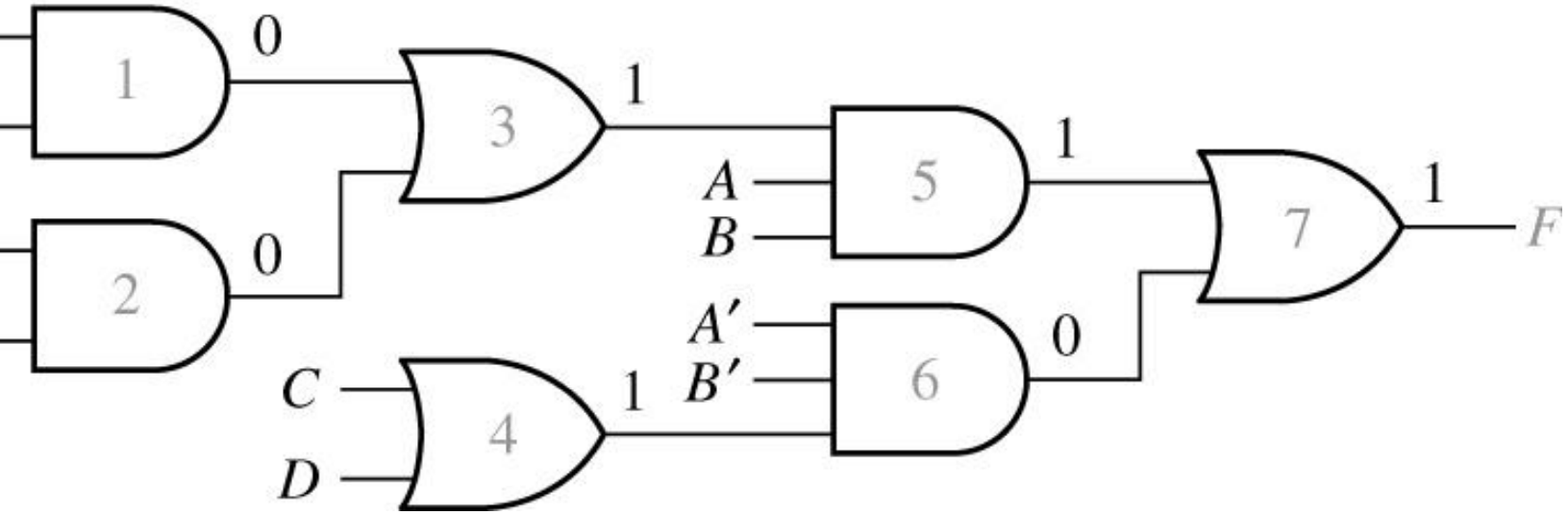


Simulation screen showing switches

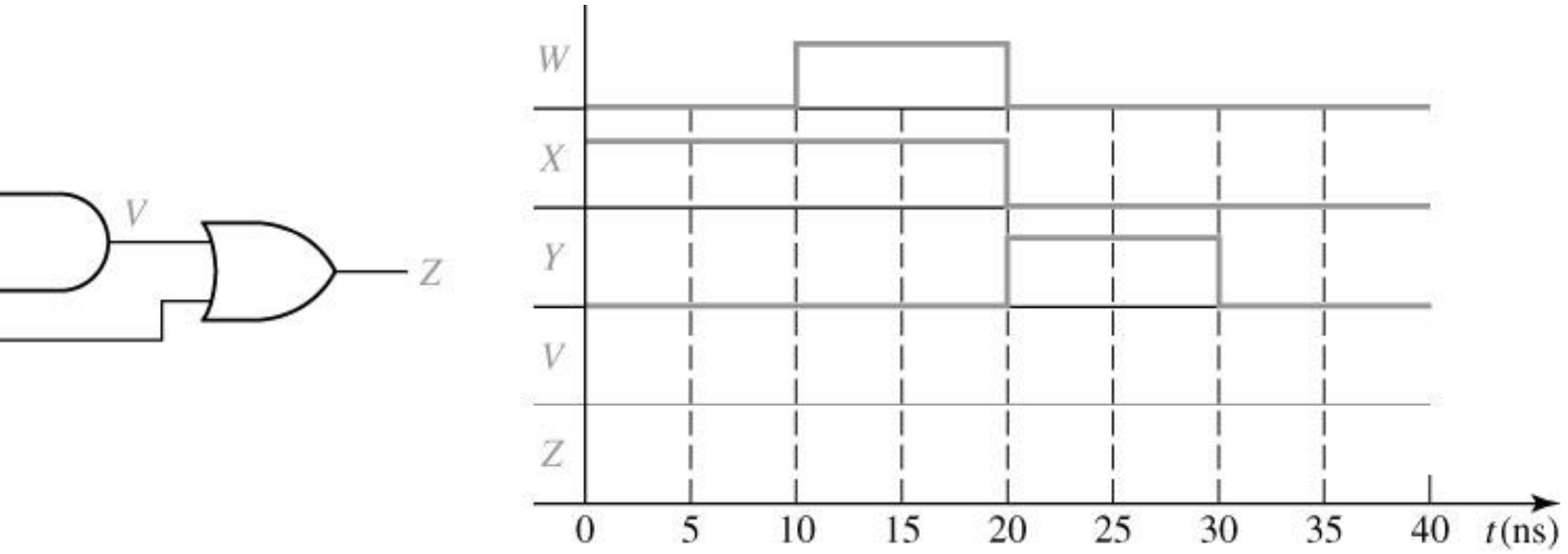


(b) Simulation screen with missing gate input

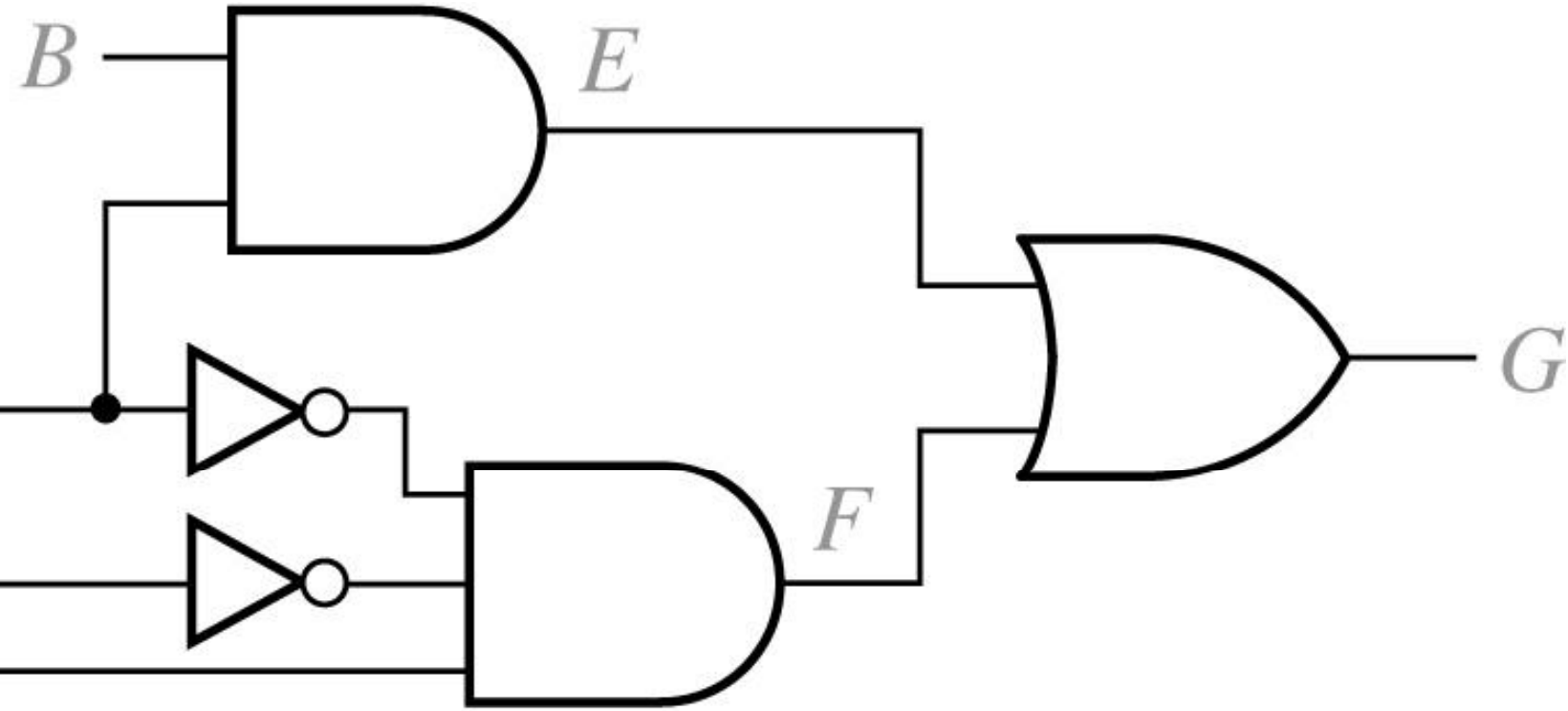
Figure 8-12



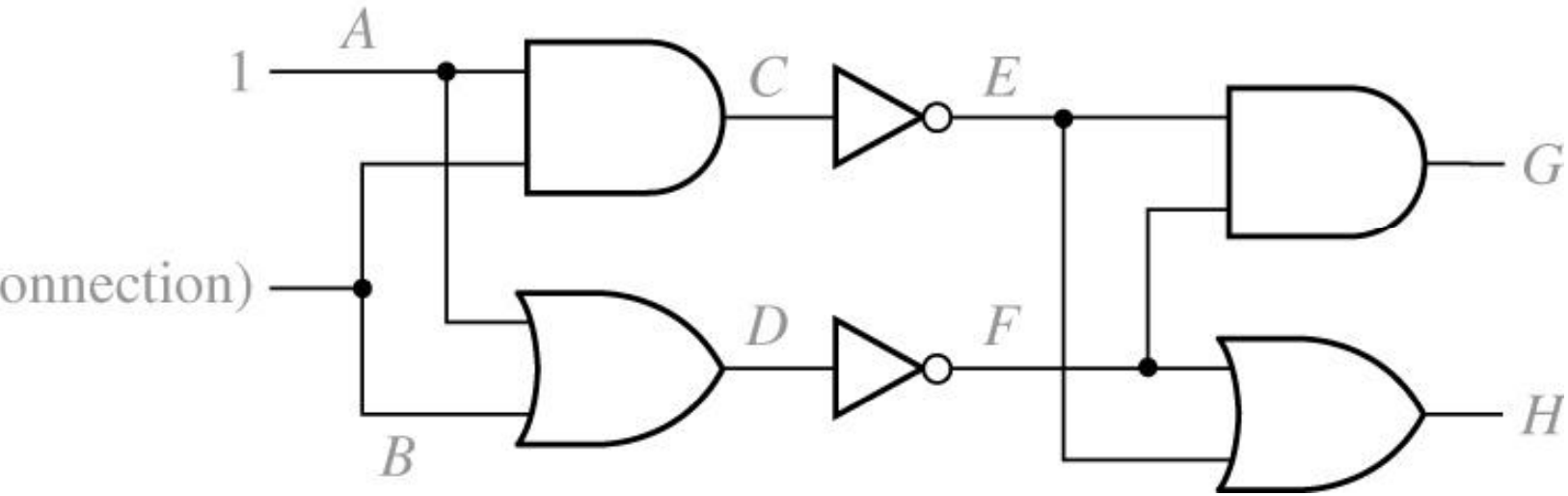
gure 8-13: Logic Circuit with Incorrect Output



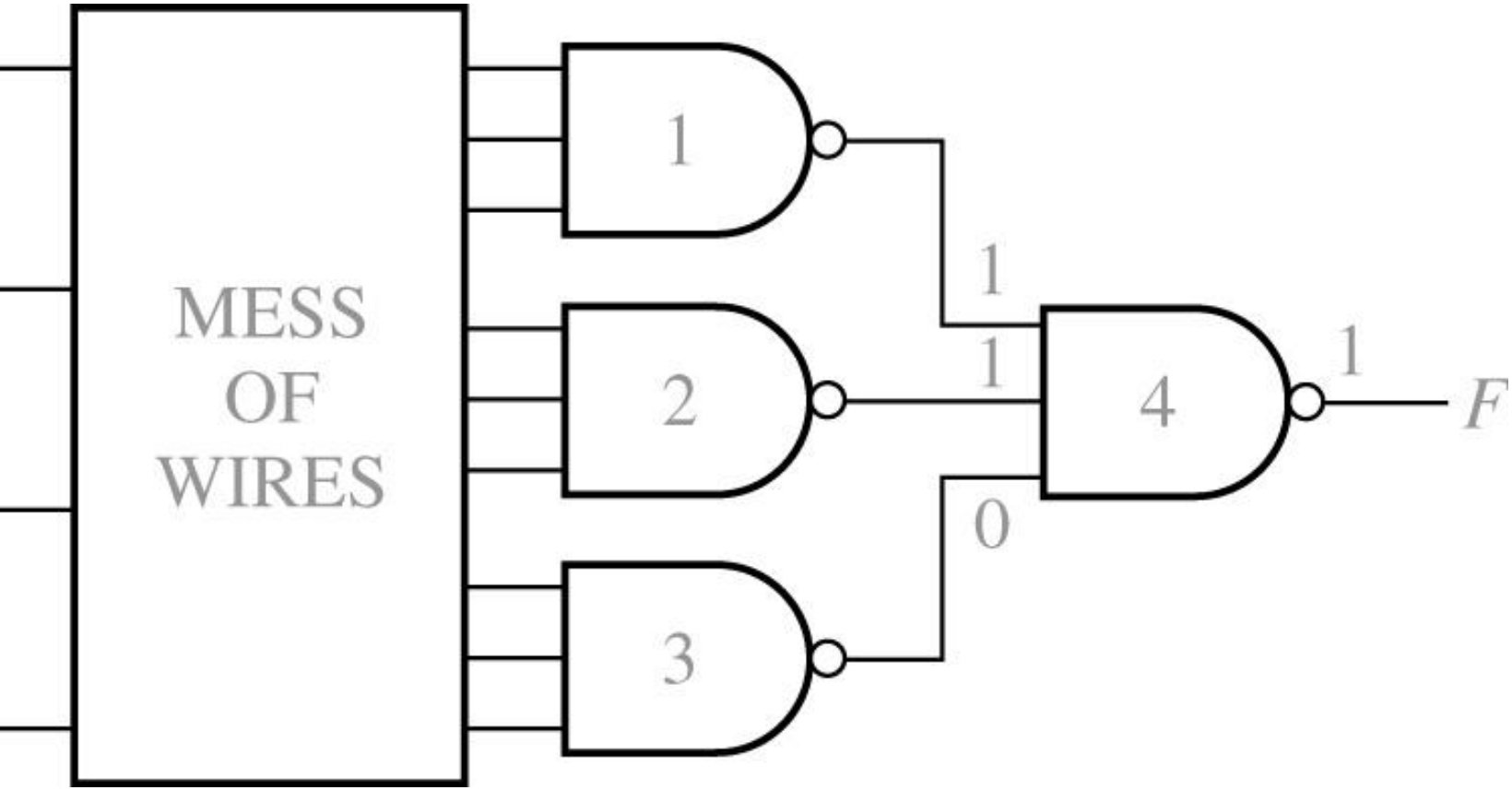
Problem 8.1



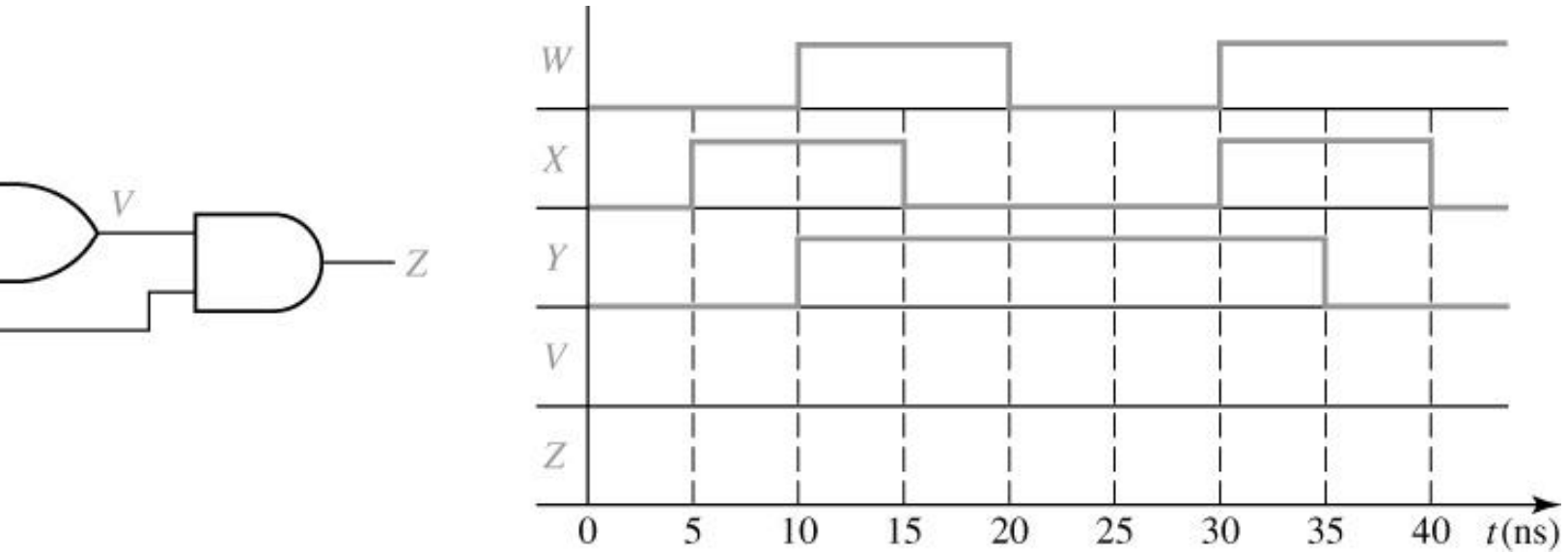
Problem 8.3



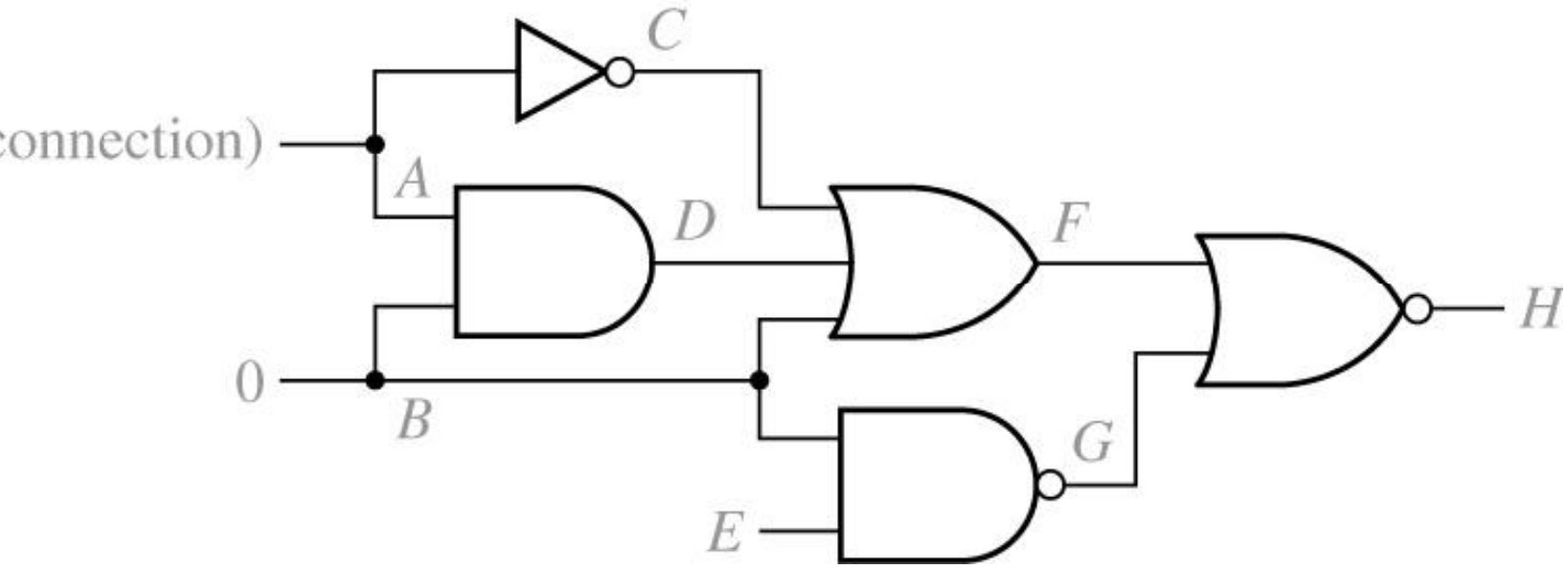
Problem 8.4



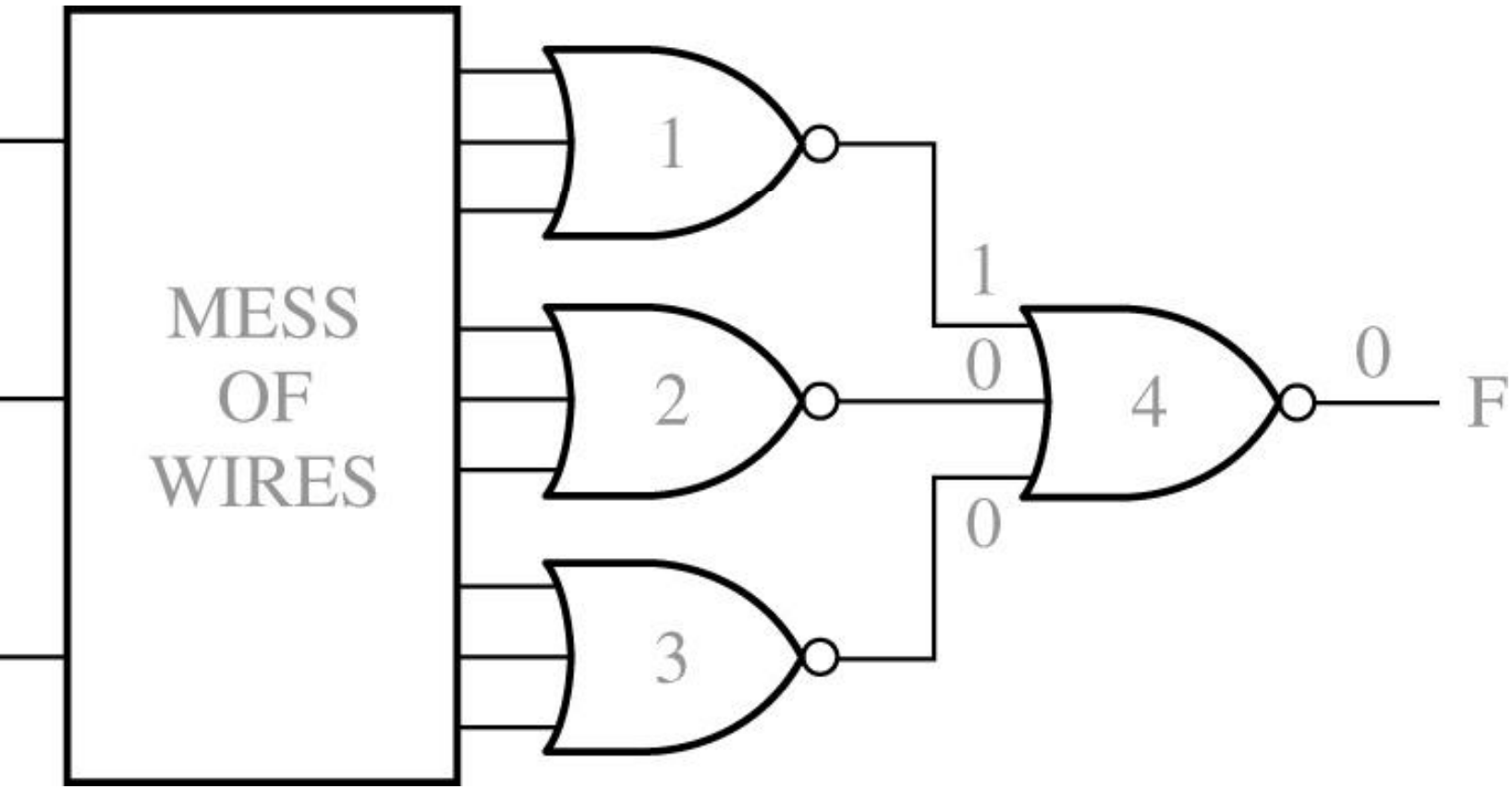
Problem 8.5



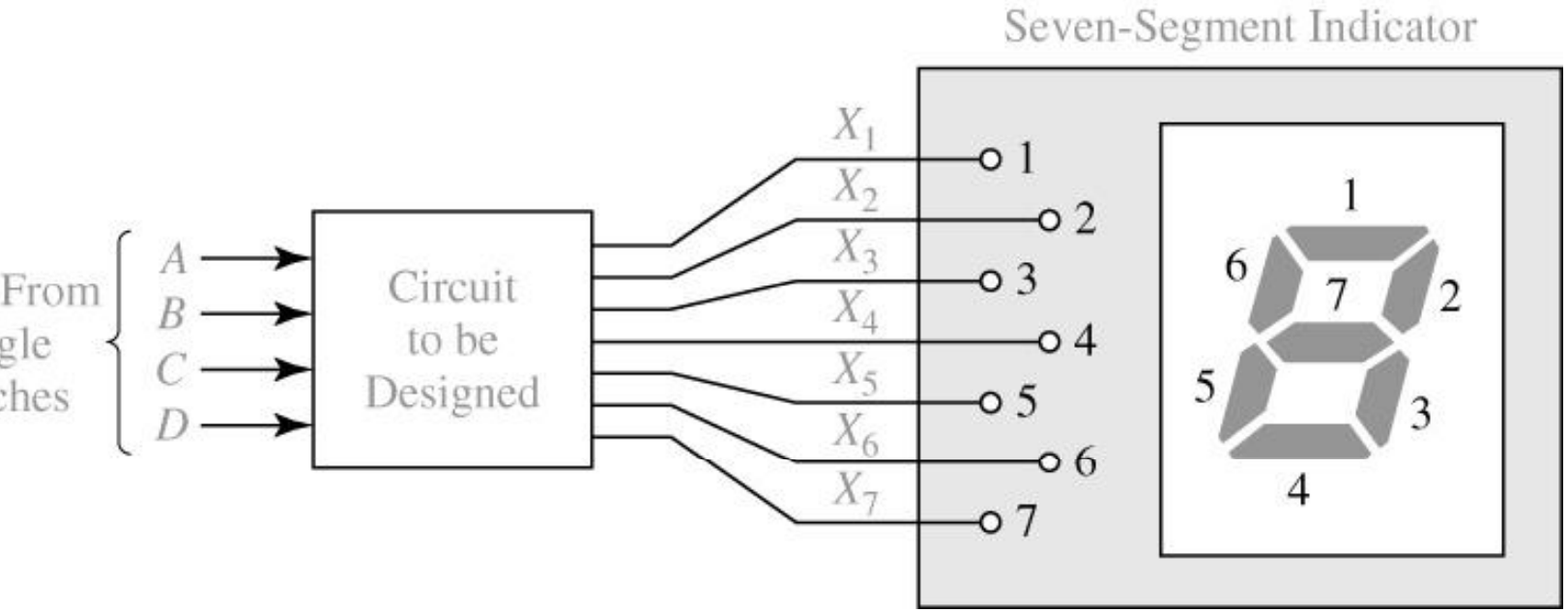
Problem 8.6



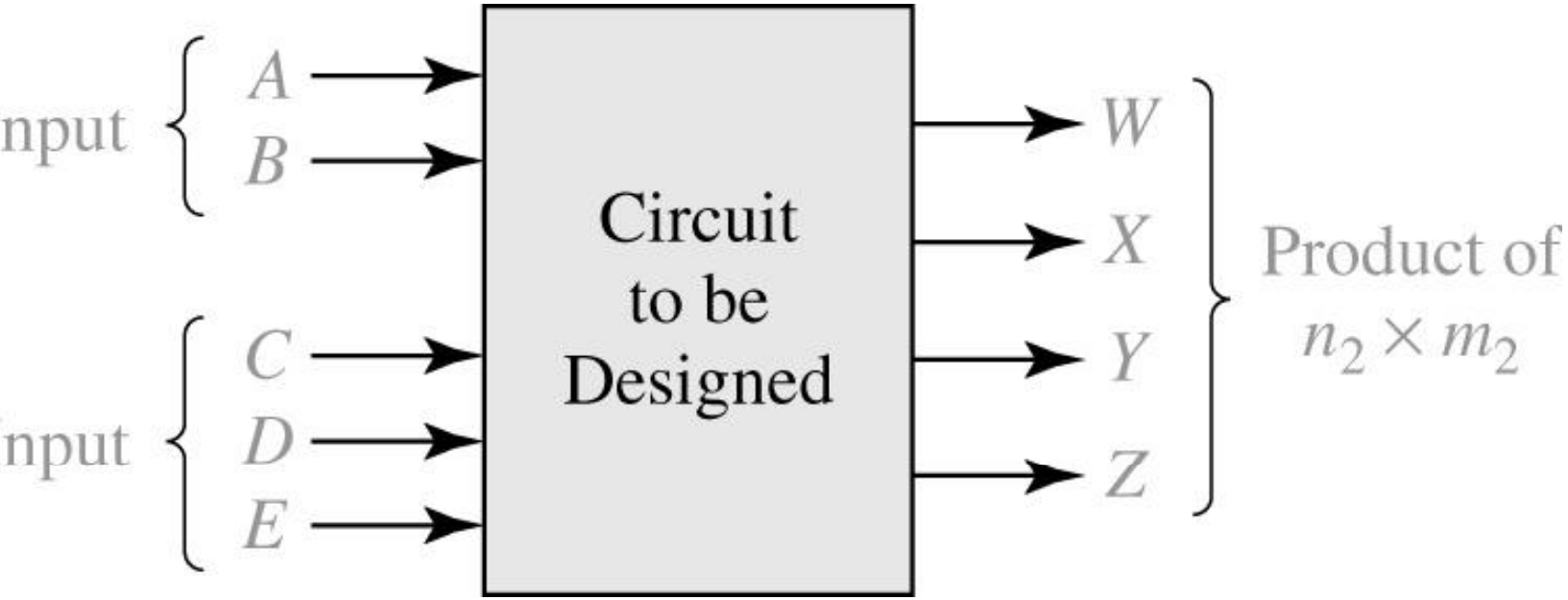
Problem 8.8



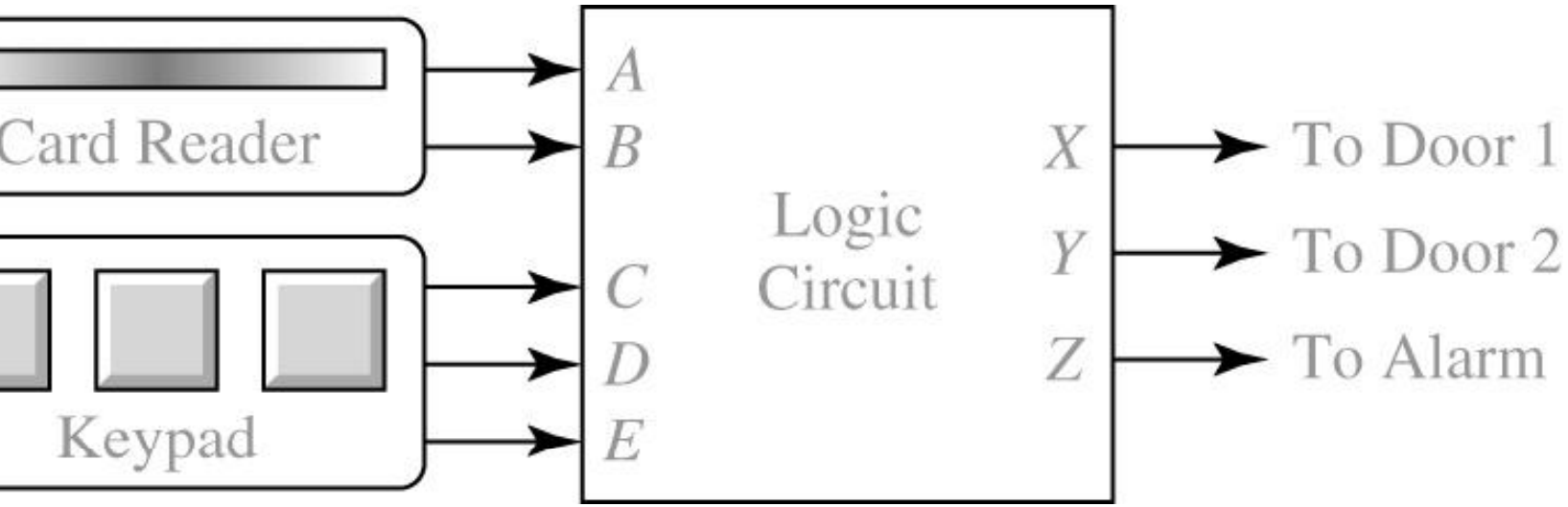
Problem 8-9



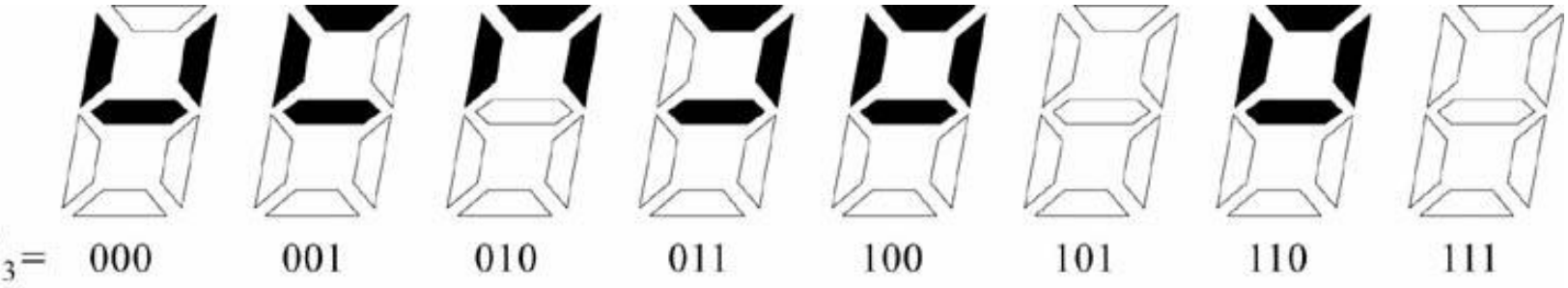
re 8.14: Circuit Driving Seven-Segment Module



Design Problem 8.C



Design Problem 8.N



Design Problem 8.S