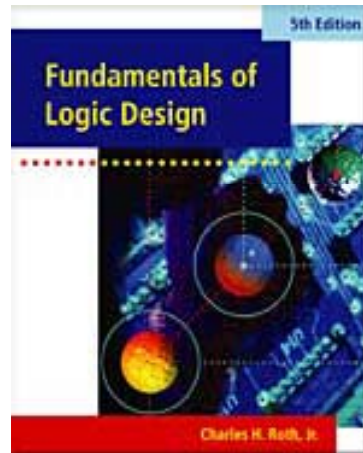


FIGURES FOR
CHAPTER 13

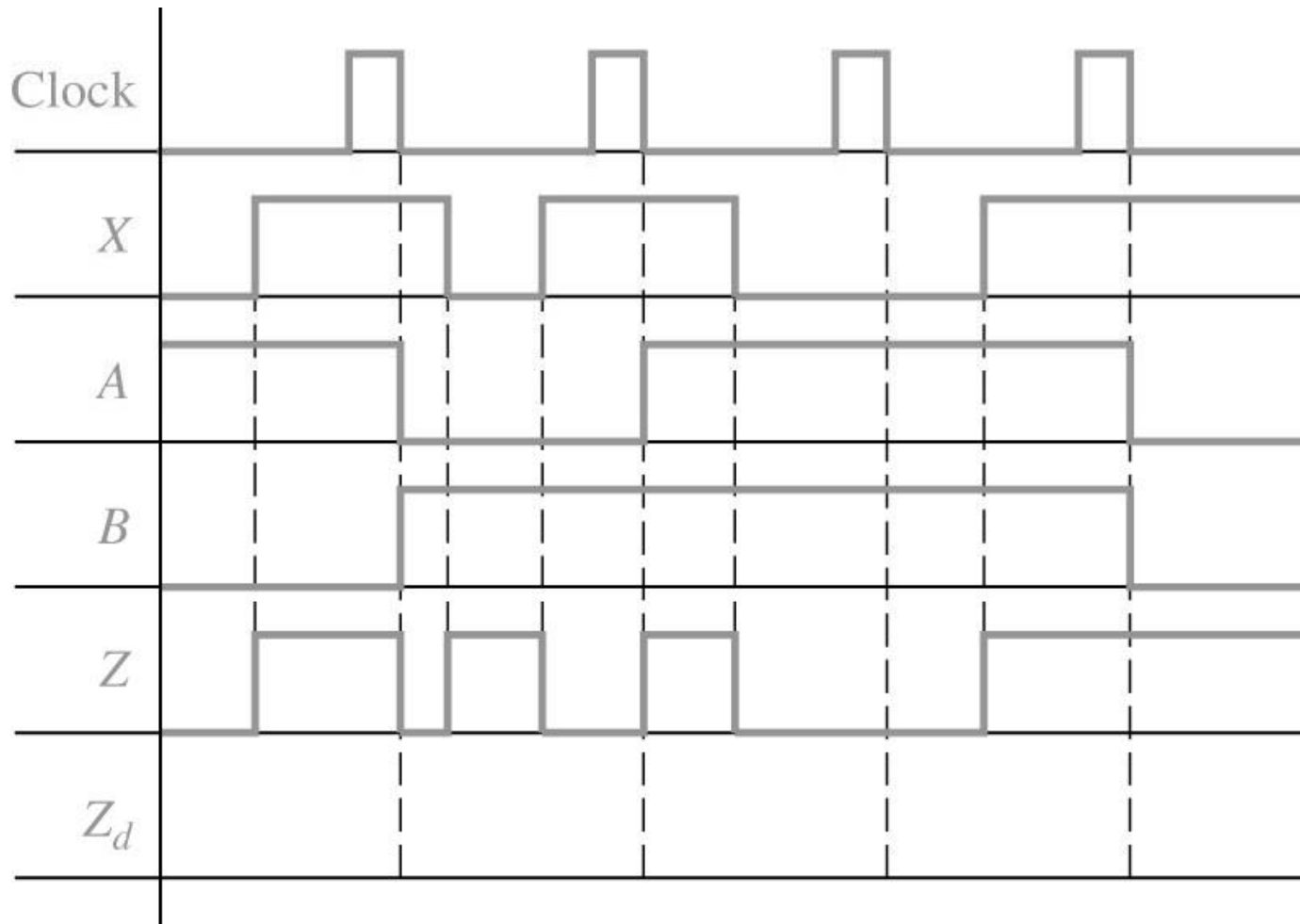
**ANALYSIS OF CLOCKED
SEQUENTIAL CIRCUITS**



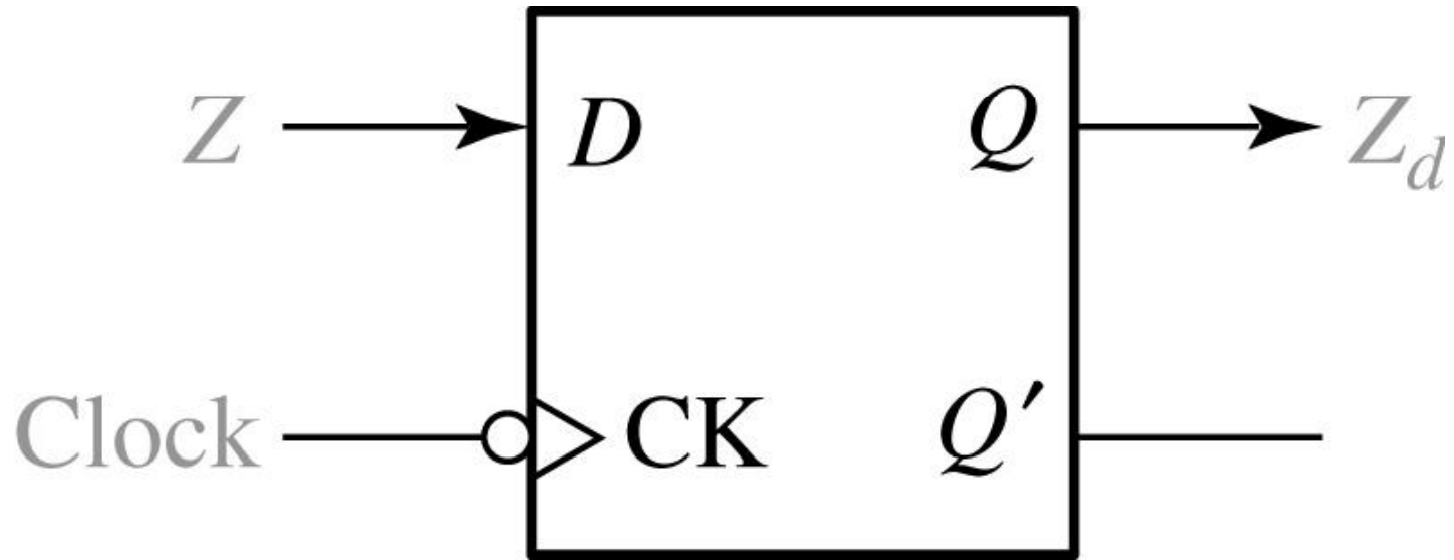
This chapter in the book includes:

- Objectives
- Study Guide
- 13.1 A Sequential Parity Checker
- 13.2 Analysis by Signal Tracing and Timing Charts
- 13.3 State Tables and Graphs
- 13.4 General Models for Sequential Circuits
- Programmed Exercise
- Problems

Click the mouse to move to the next page.
Use the ESC key to exit this chapter.



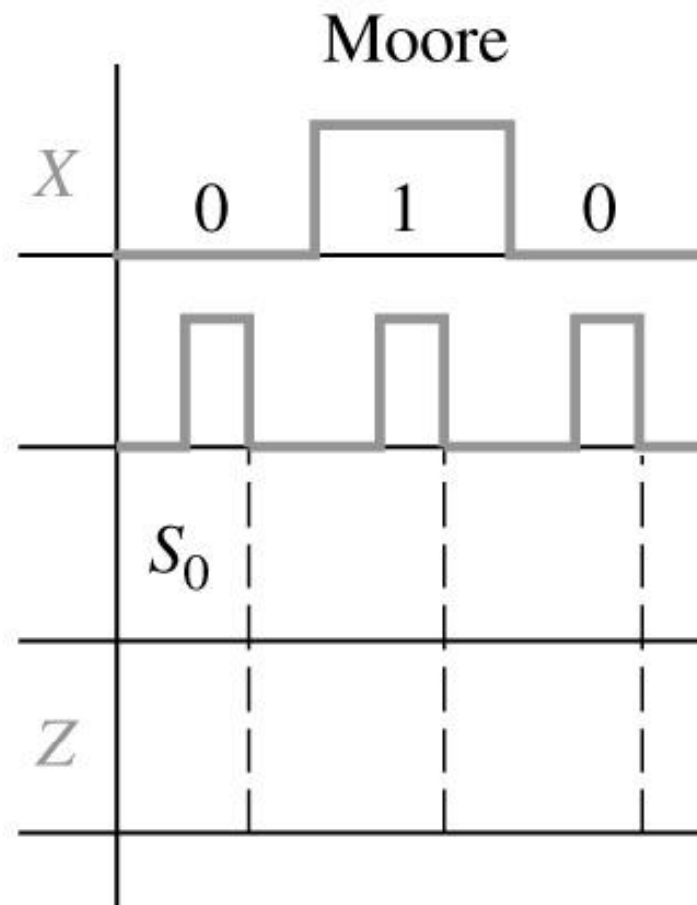
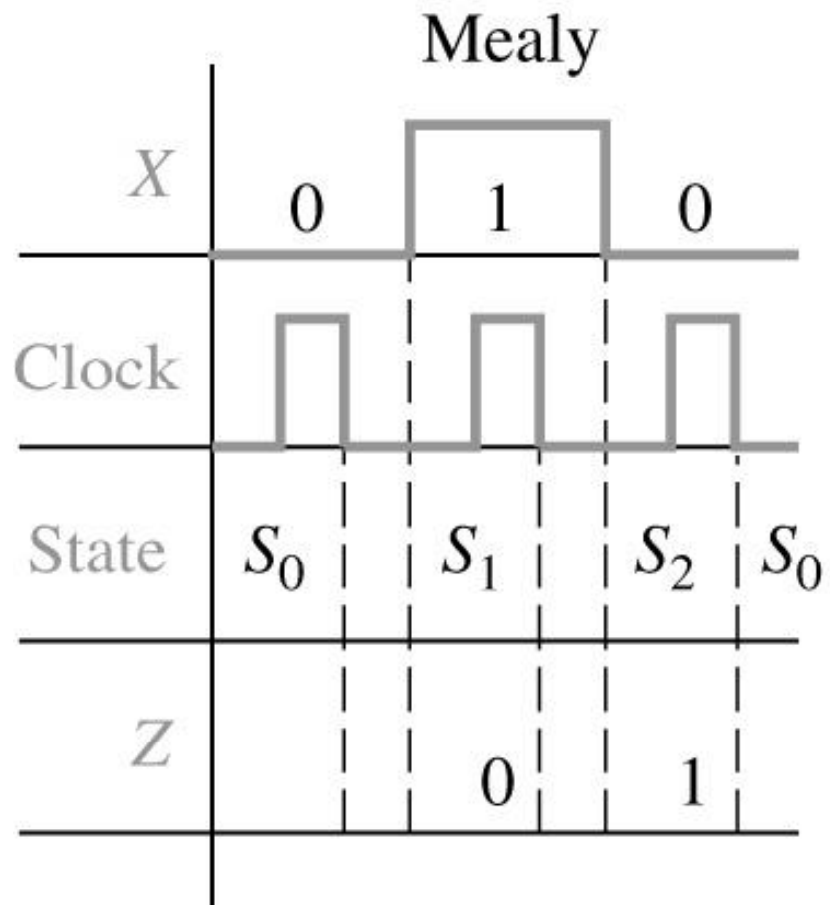
Study Guide, No. 4



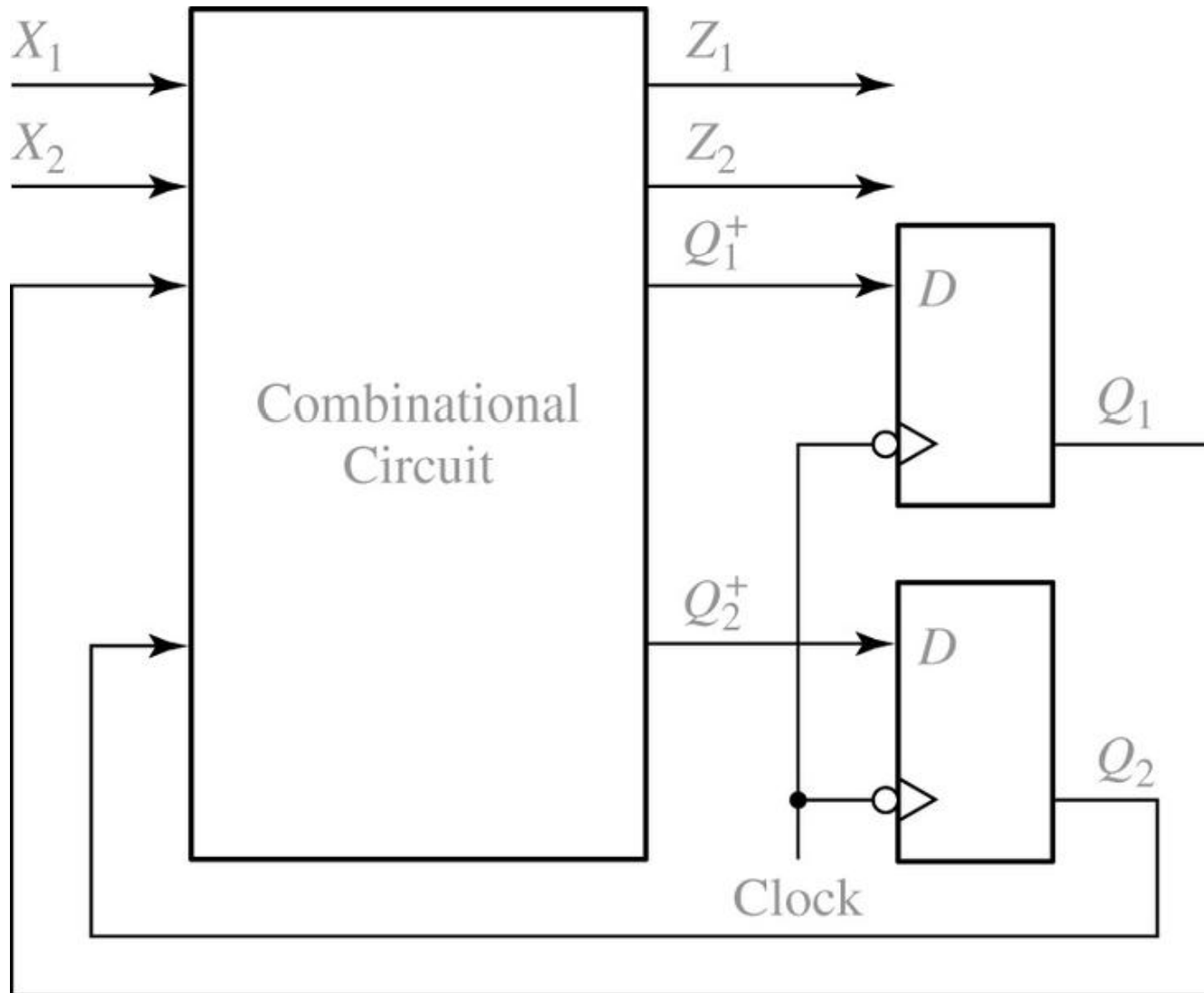
Study Guide, No. 4e



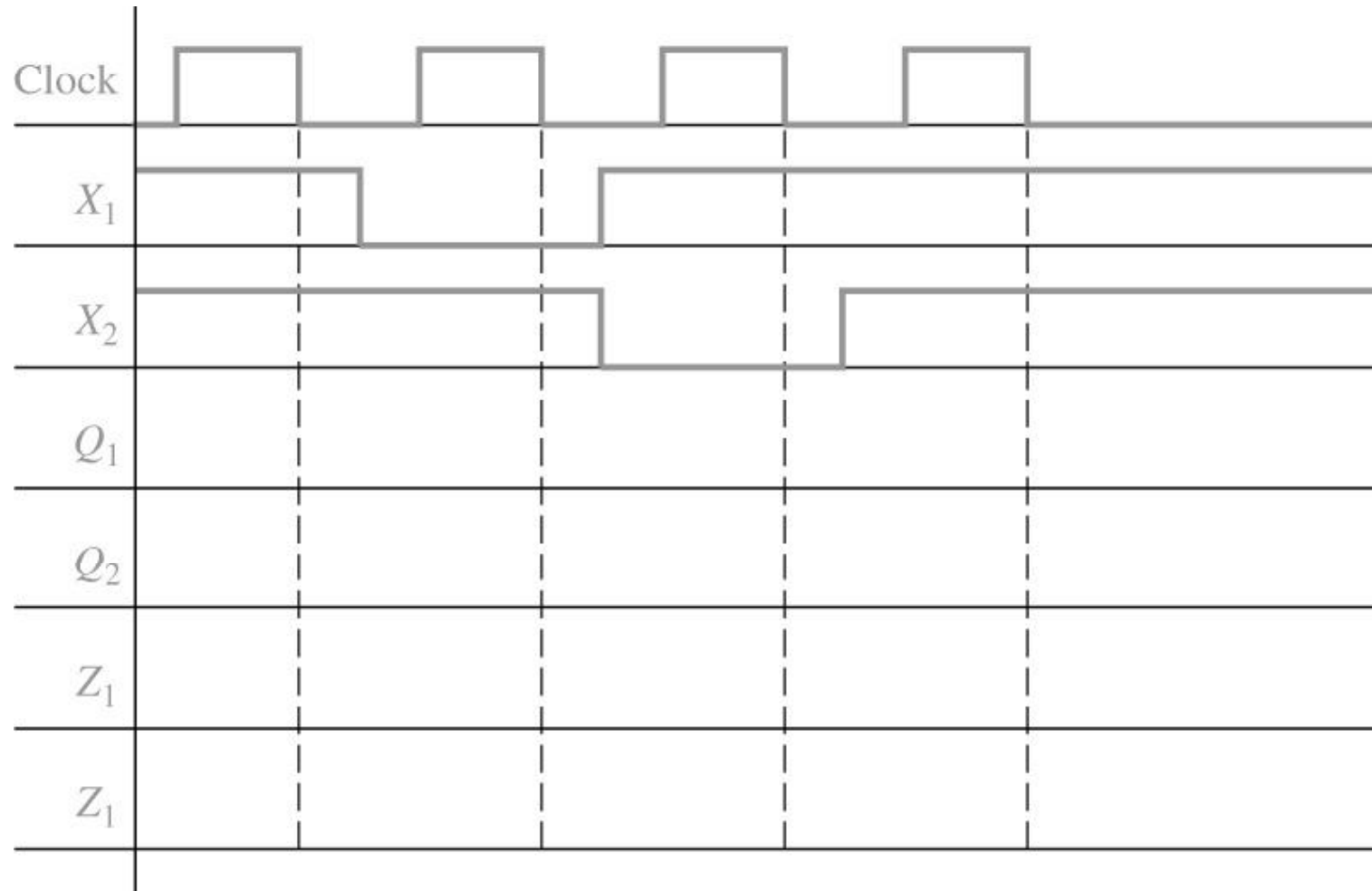
Study Guide, No. 4g



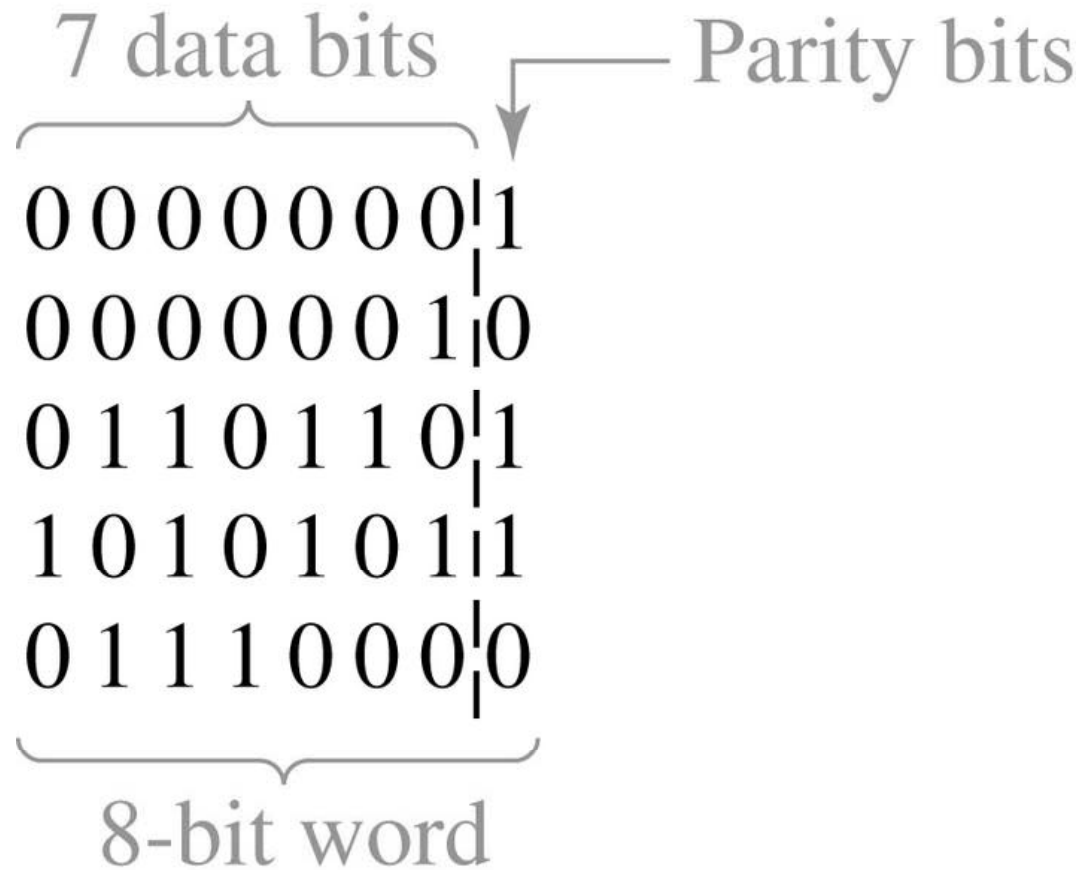
Study Guide, No. 5c



Study Guide, No. 6a



Study Guide, No. 6a6



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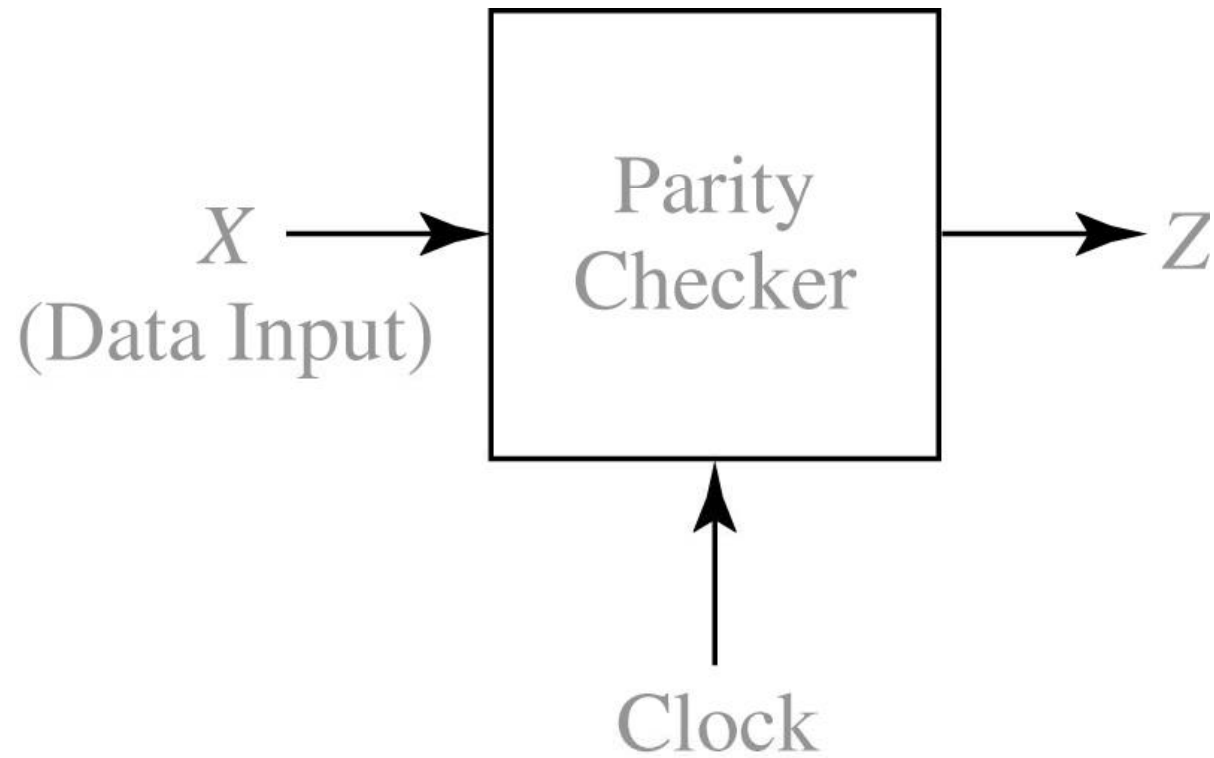


Figure 13-1: Block Diagram for Parity Checker

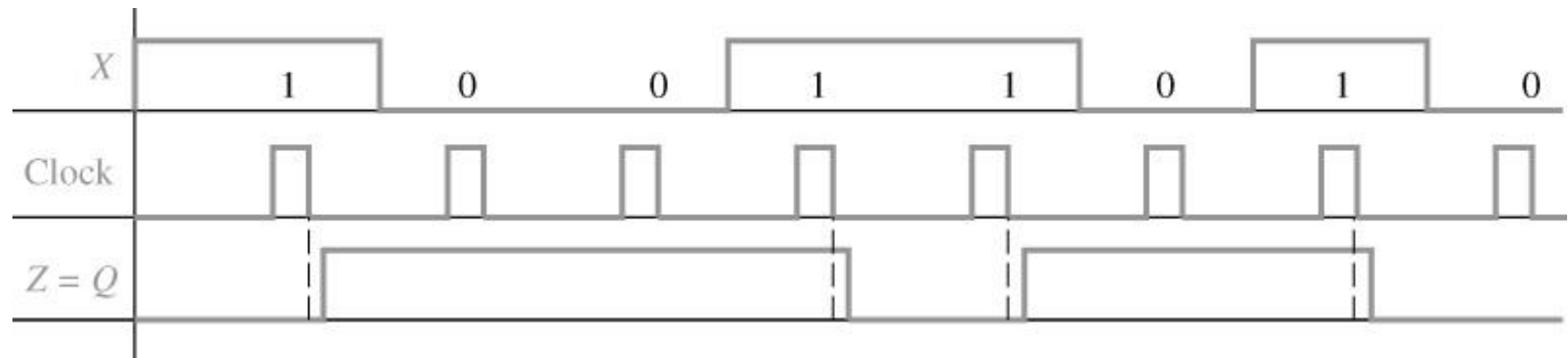


Figure 13-2: Waveforms for Parity Checker

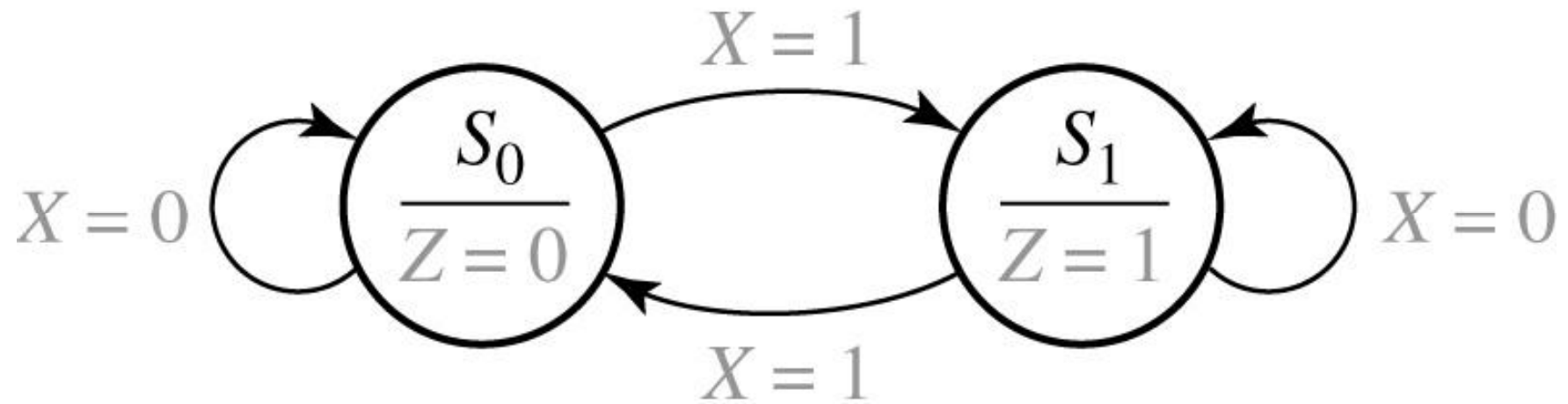


Figure 13-3: State Graph for Parity Checker

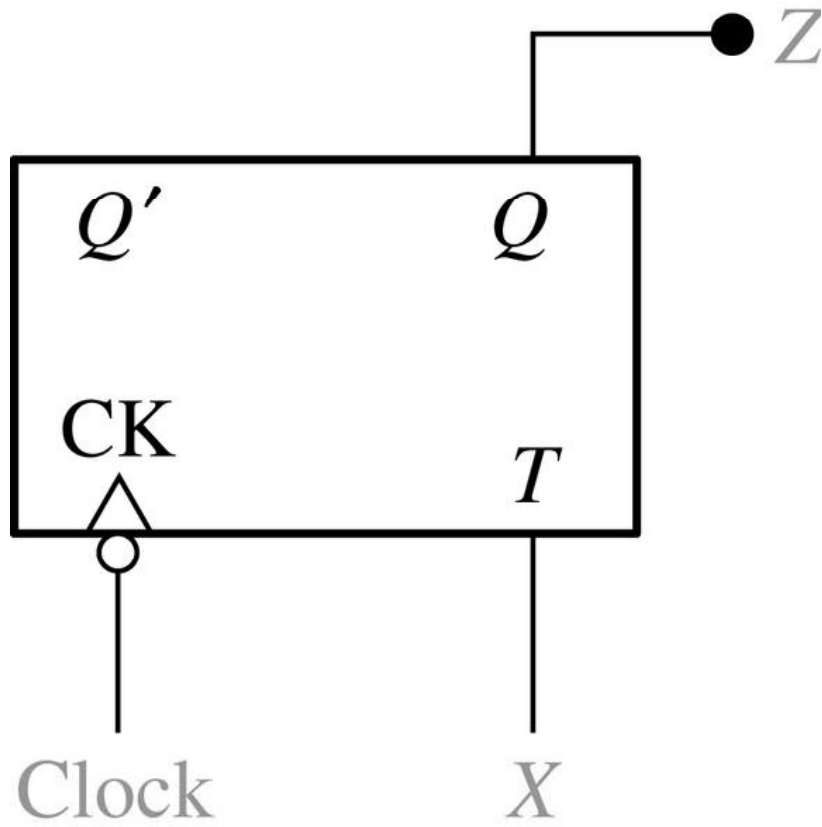


Figure 13-4: Parity Checker

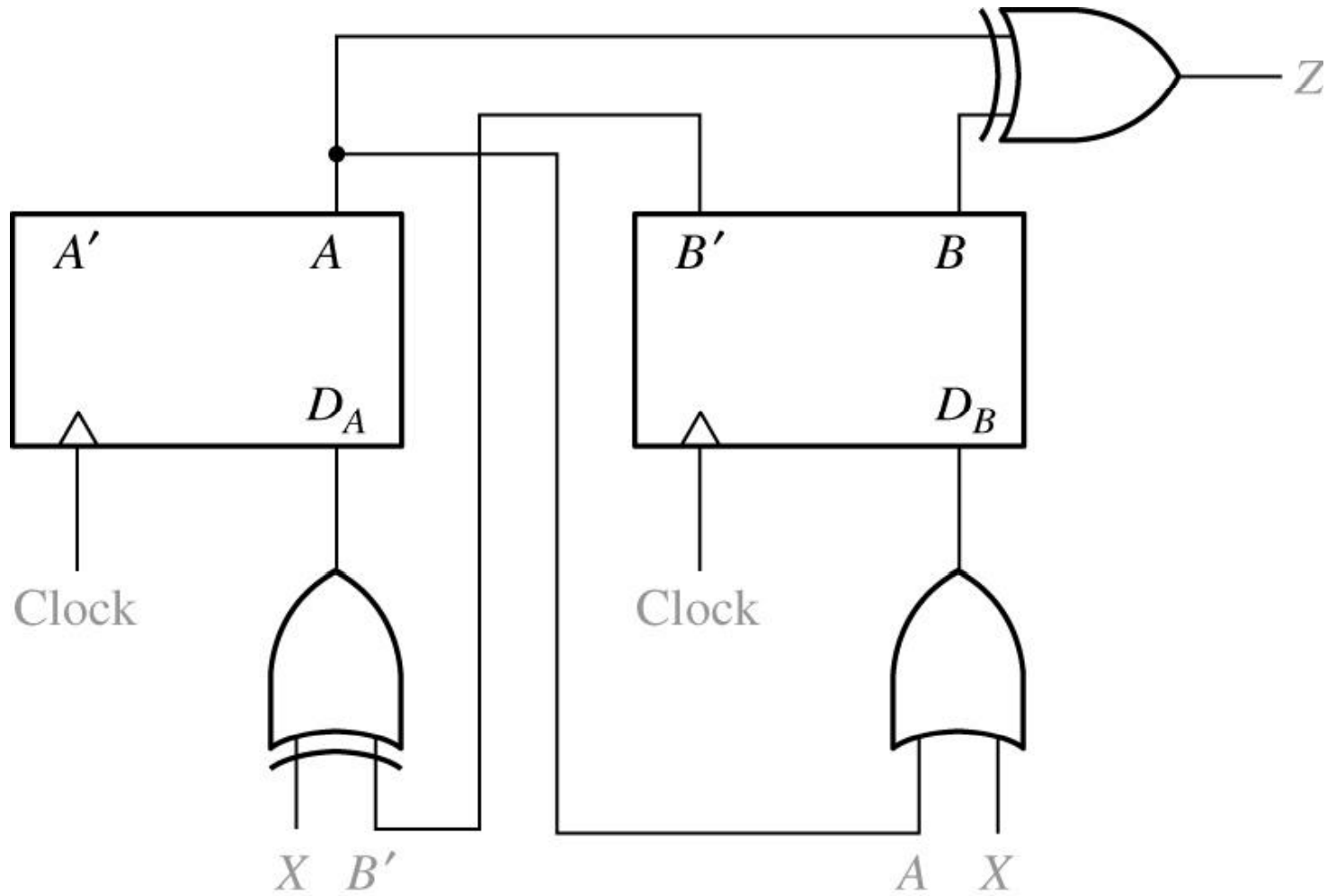


Figure 13-5: Moore Sequential Circuit to be Analyzed

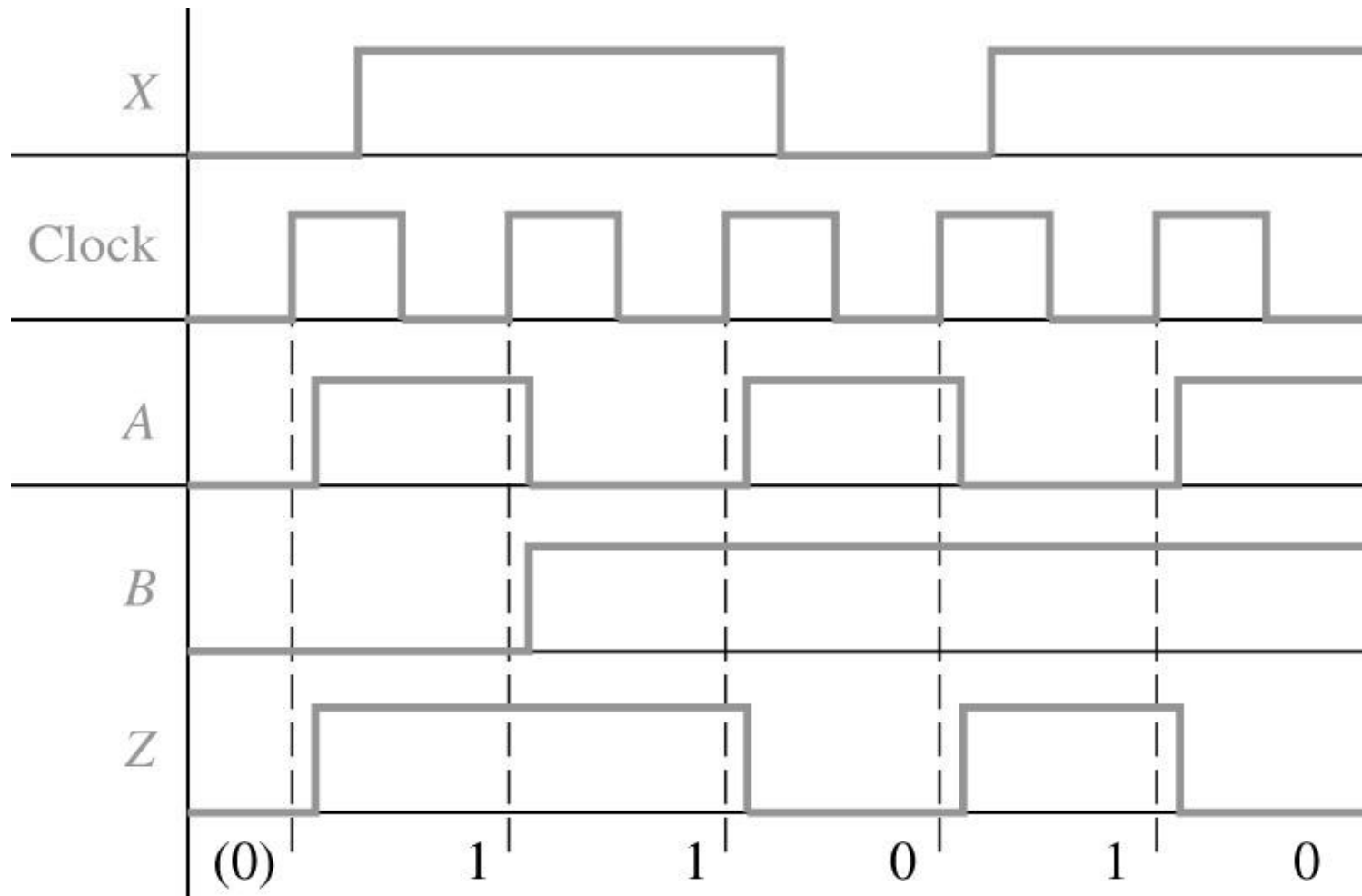


Figure 13-6: Timing Chart for Figure 13-5

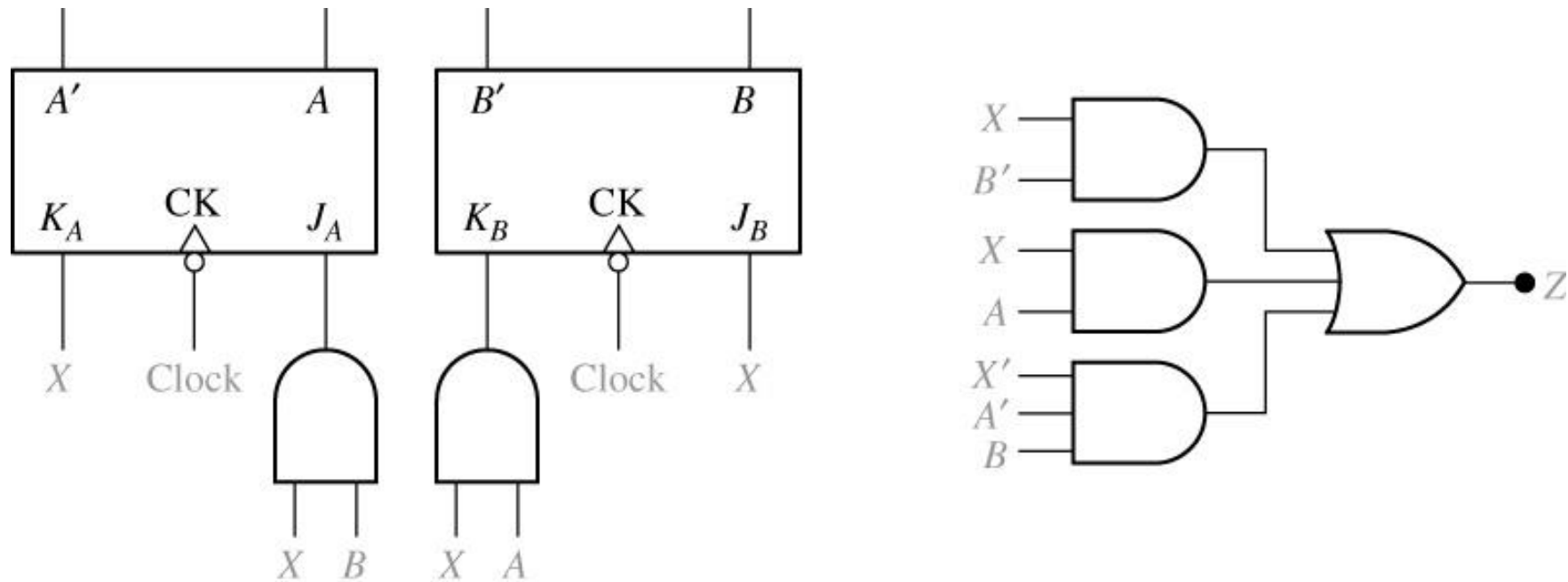


Figure 13-7: Mealy Sequential Circuit to be Analyzed

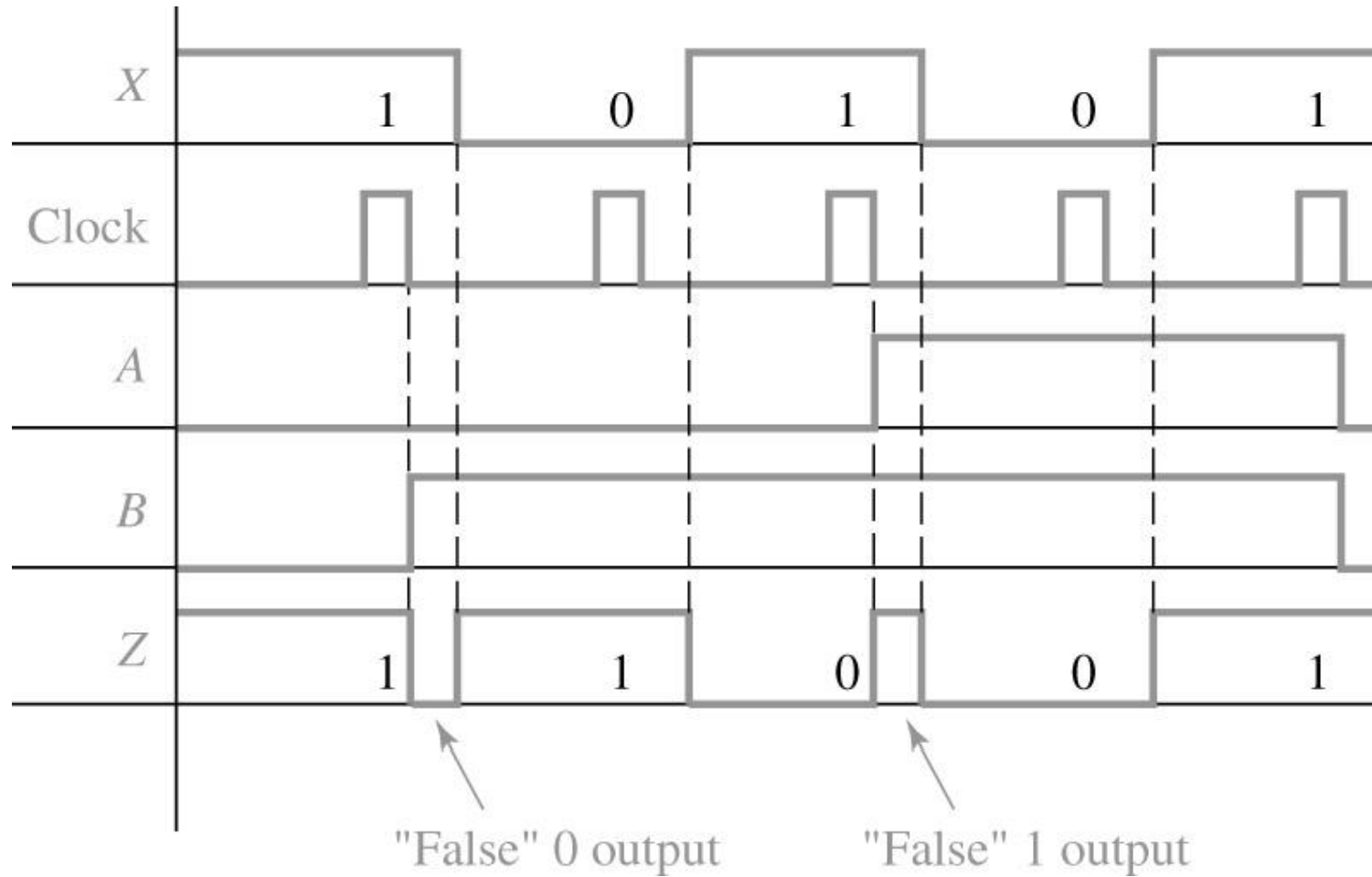


Figure 13-8: Timing Chart for Circuit of Figure 13-7

	X		
AB		0	1
00		1	0
01		0	1
11		0	1
10		1	0
		A^+	

	X		
AB		0	1
00		0	1
01		0	1
11		1	1
10		1	1
		B^+	

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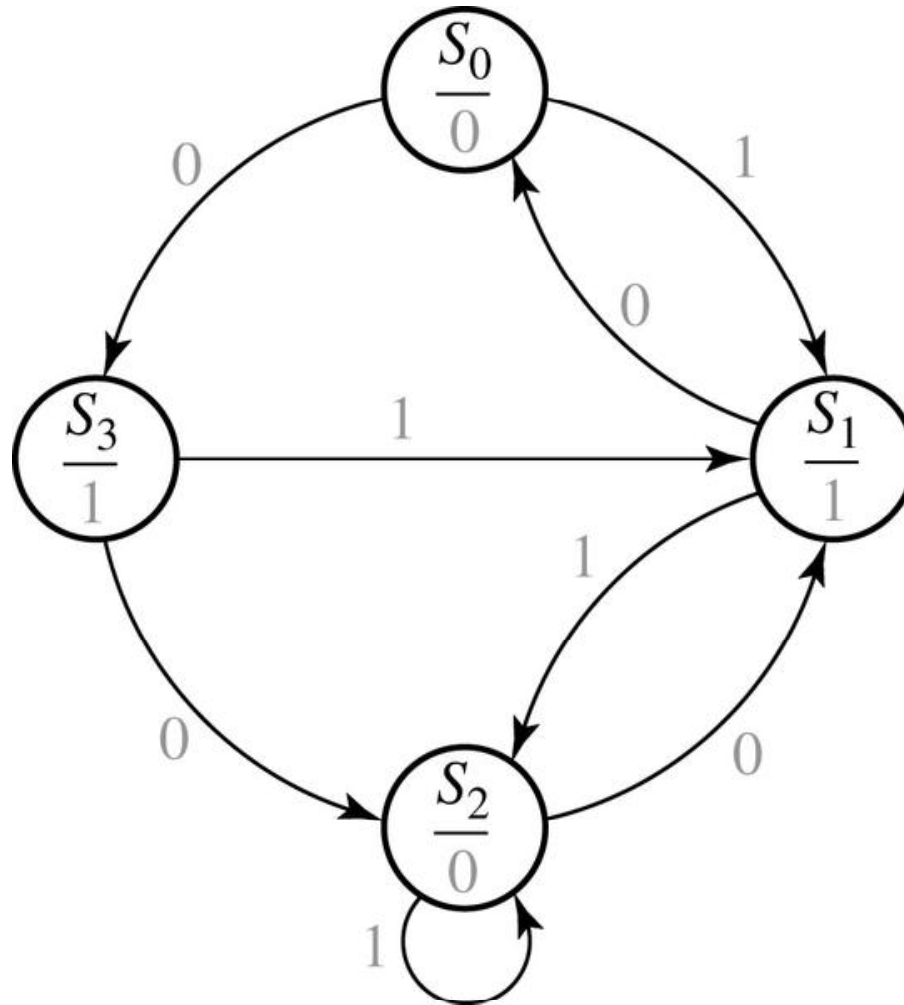


Figure 13-9: Moore State Graph for Figure 13-5

	X		
AB		0	1
00		0	0
01		0	1
11		1	0
10		1	0
		A^+	

	X		
AB		0	1
00		0	1
01		1	1
11		1	0
10		0	1
		B^+	

	X		
AB		0	1
00		0	1
01		1	0
11		0	1
10		0	1
		Z	

Figure 13-10

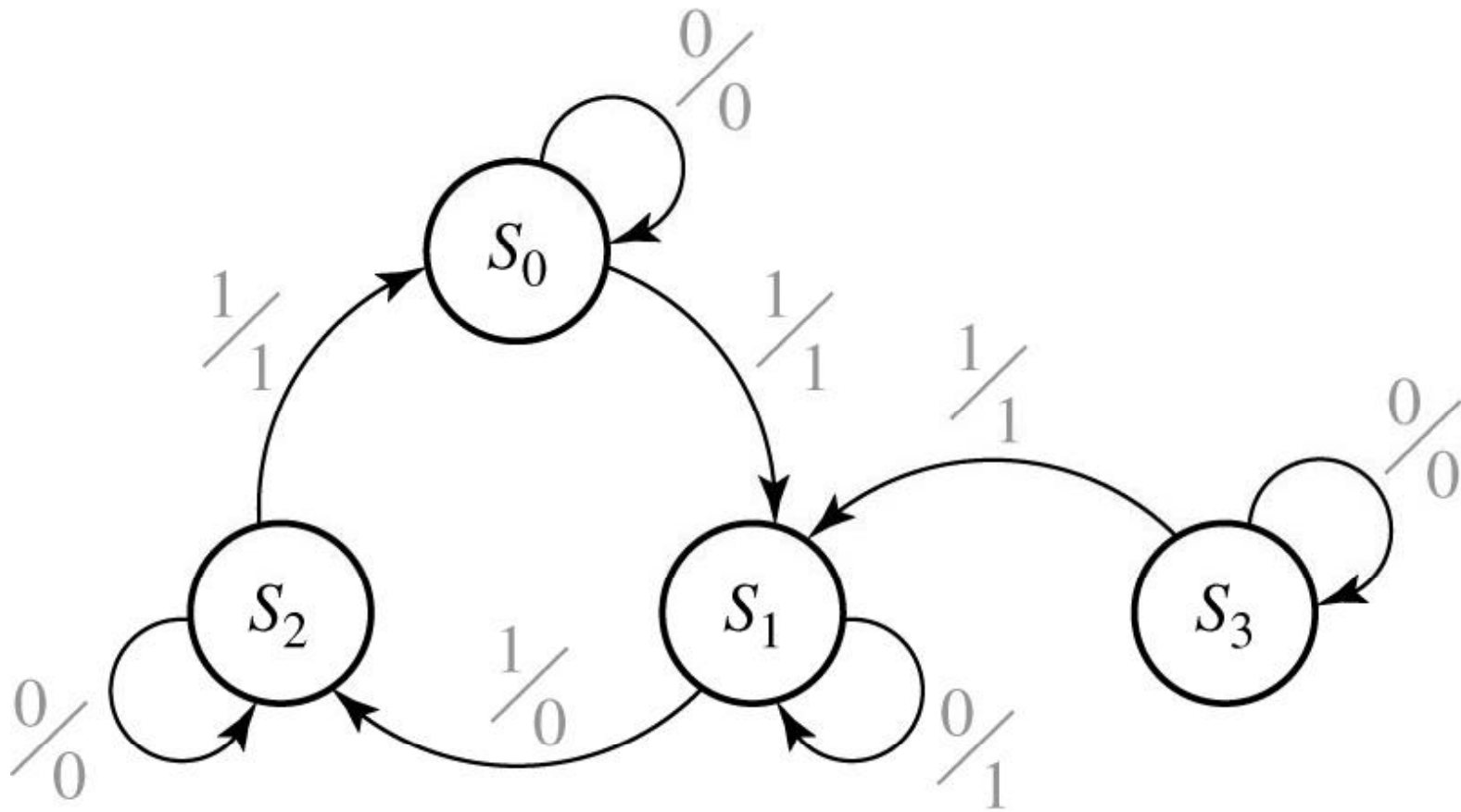
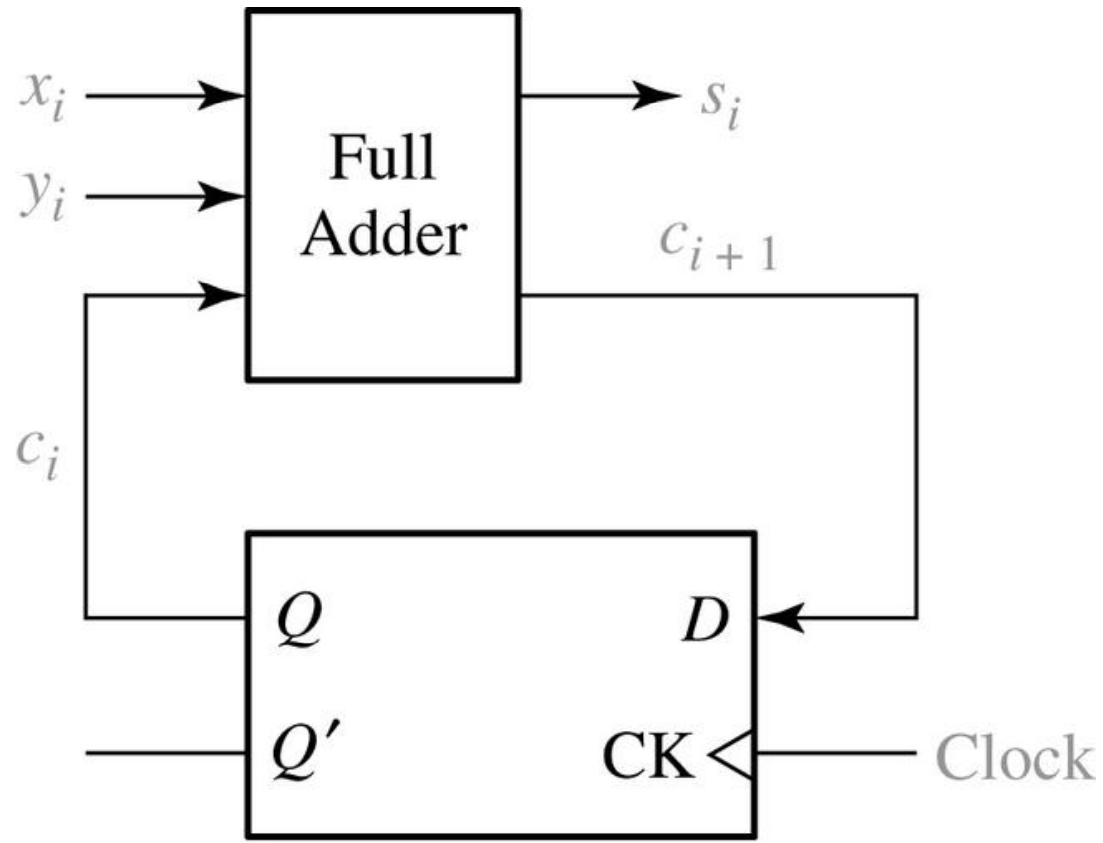


Figure 13-11: Mealy State Graph for Figure 13-7



(a) With D flip-flop

Figure 13-12a: Serial Adder

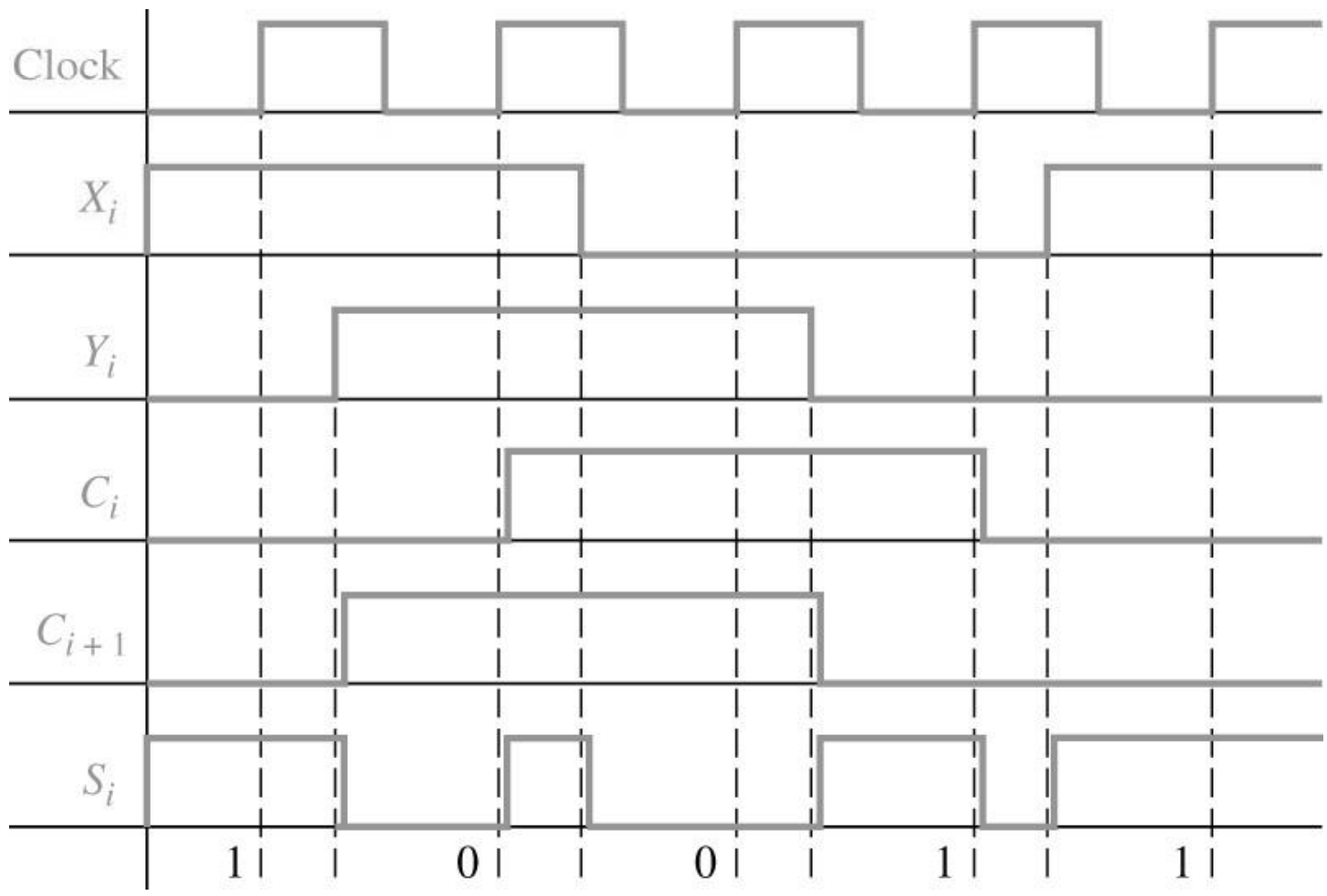


Figure 13-13: Timing Diagram for Serial Adder

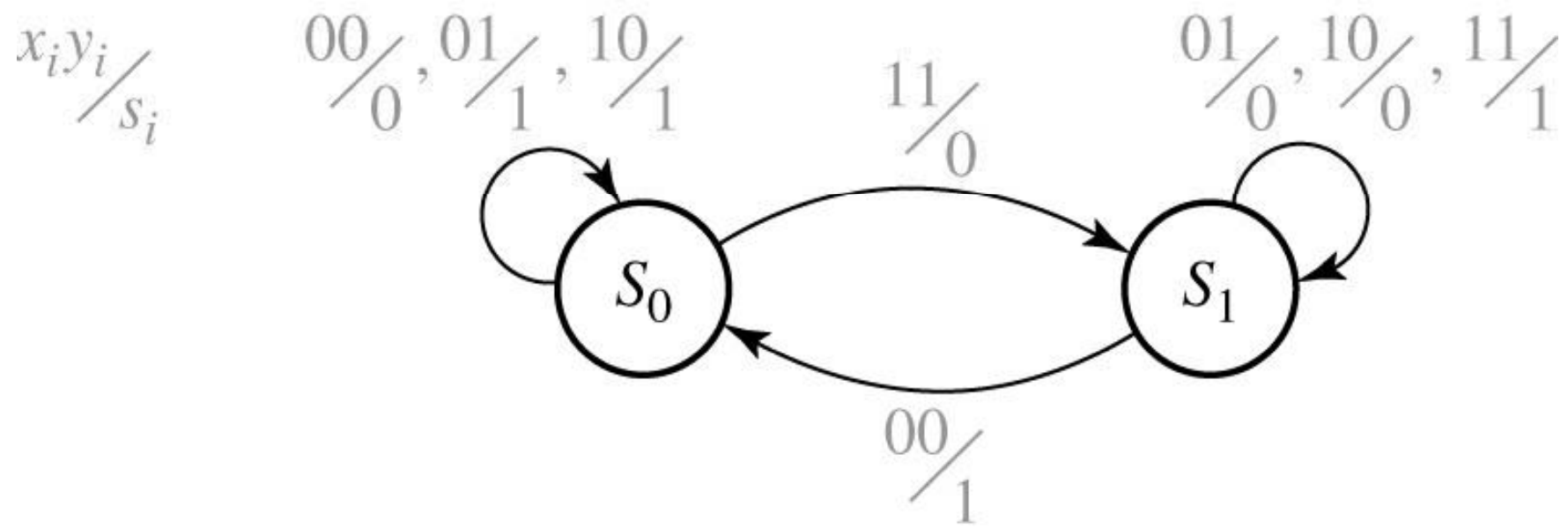


Figure 13-14: State Graph for Serial Adder

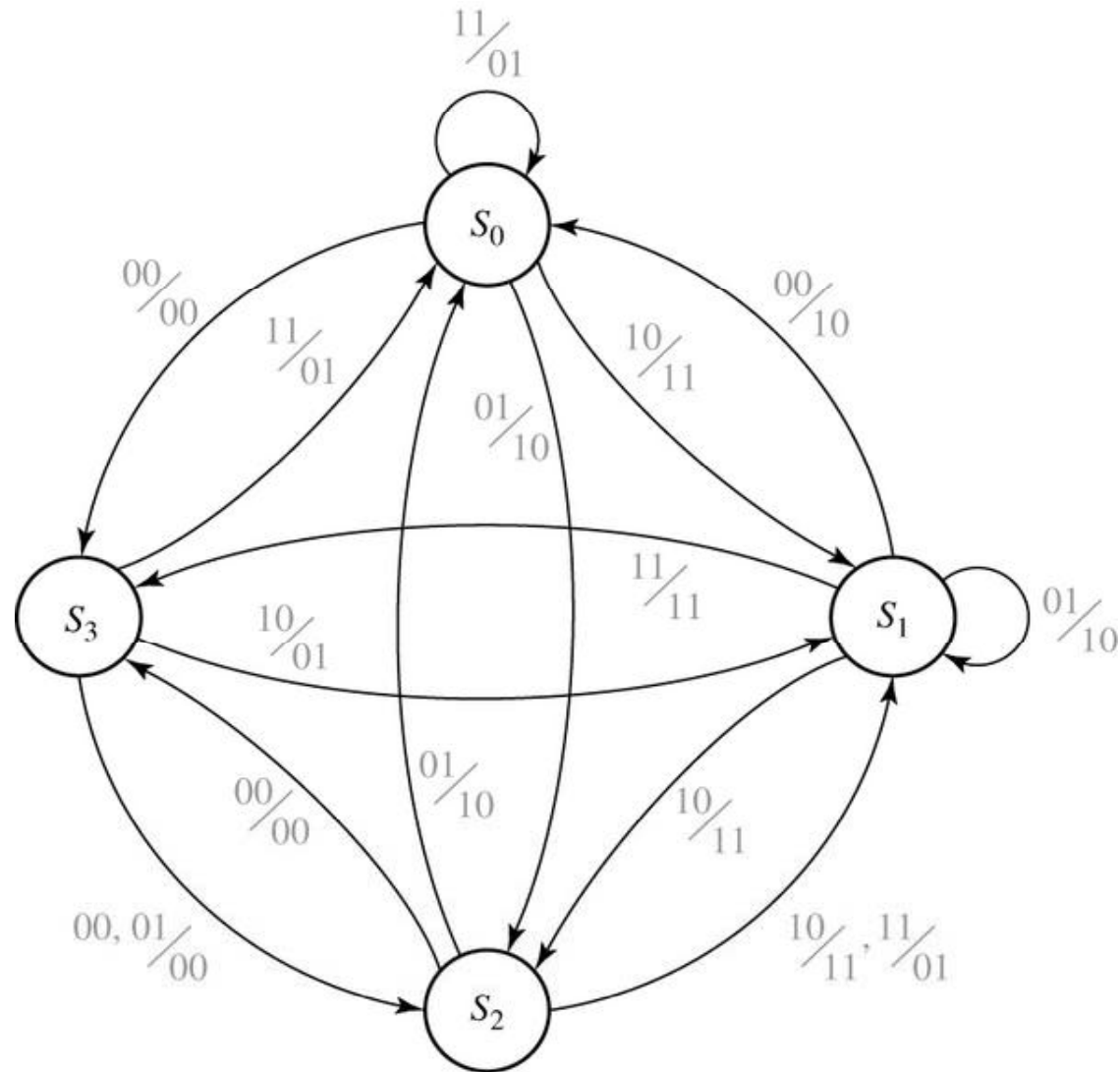
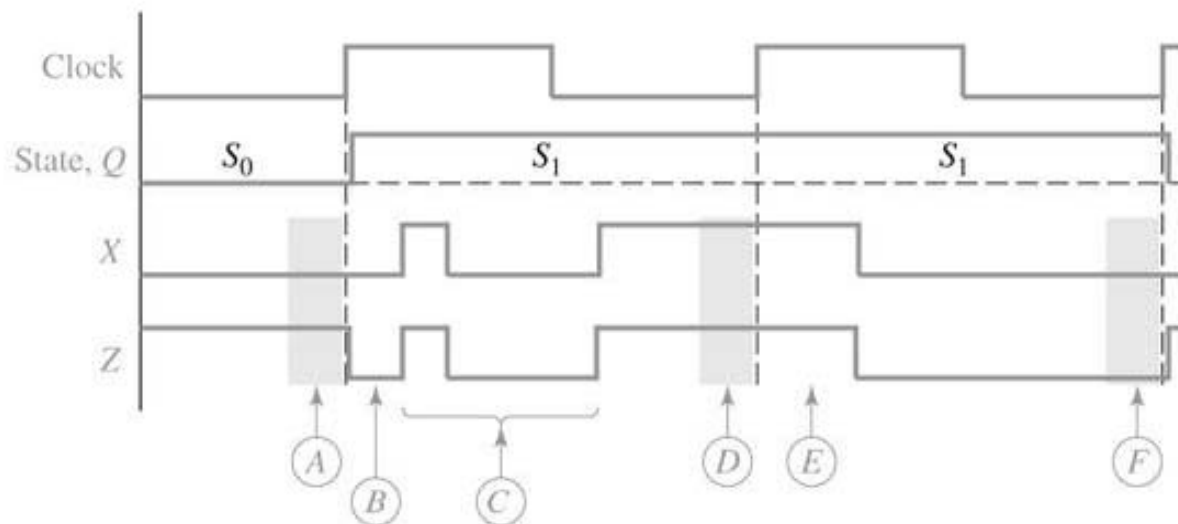
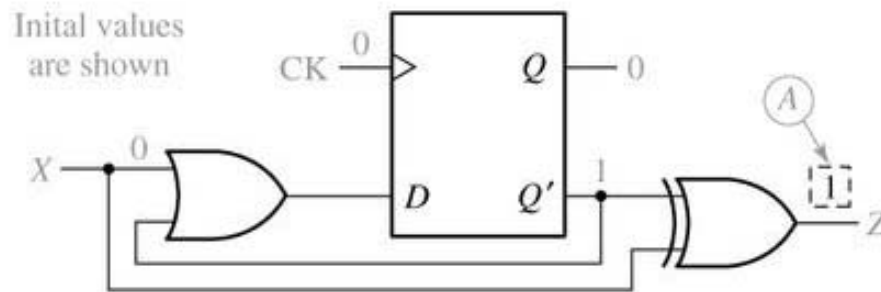
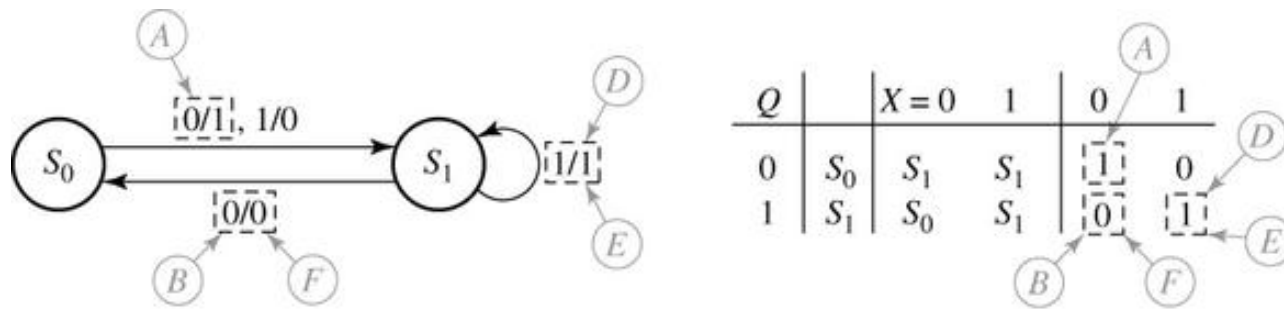


Figure 13-15: State Graph for Table 13-4



Read X and Z in shaded area (before rising edge of clock).

Figure 13-16

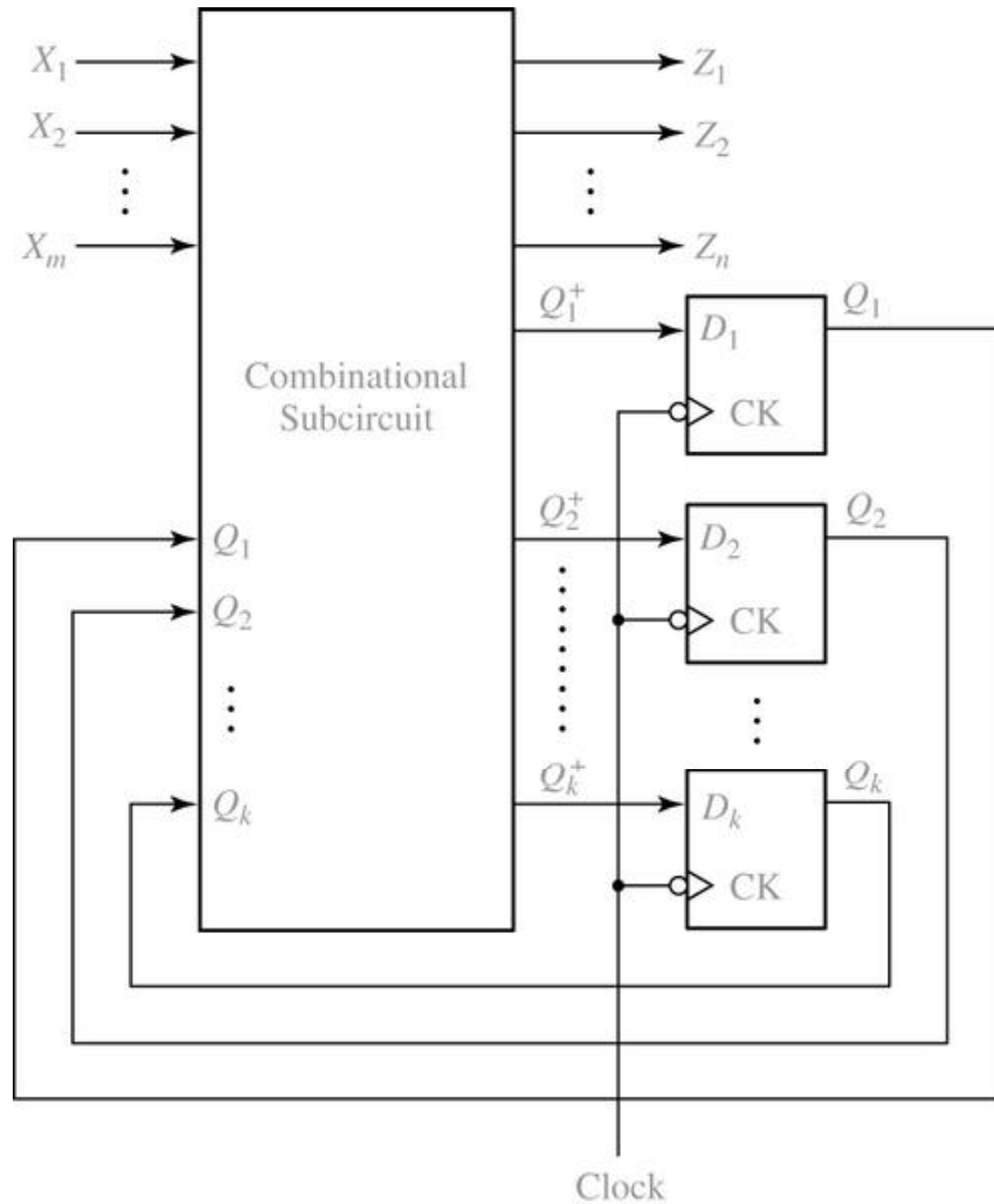


Figure 13-17:
**General Model
 for Mealy Circuit
 Using Clocked
 D Flip-Flops**

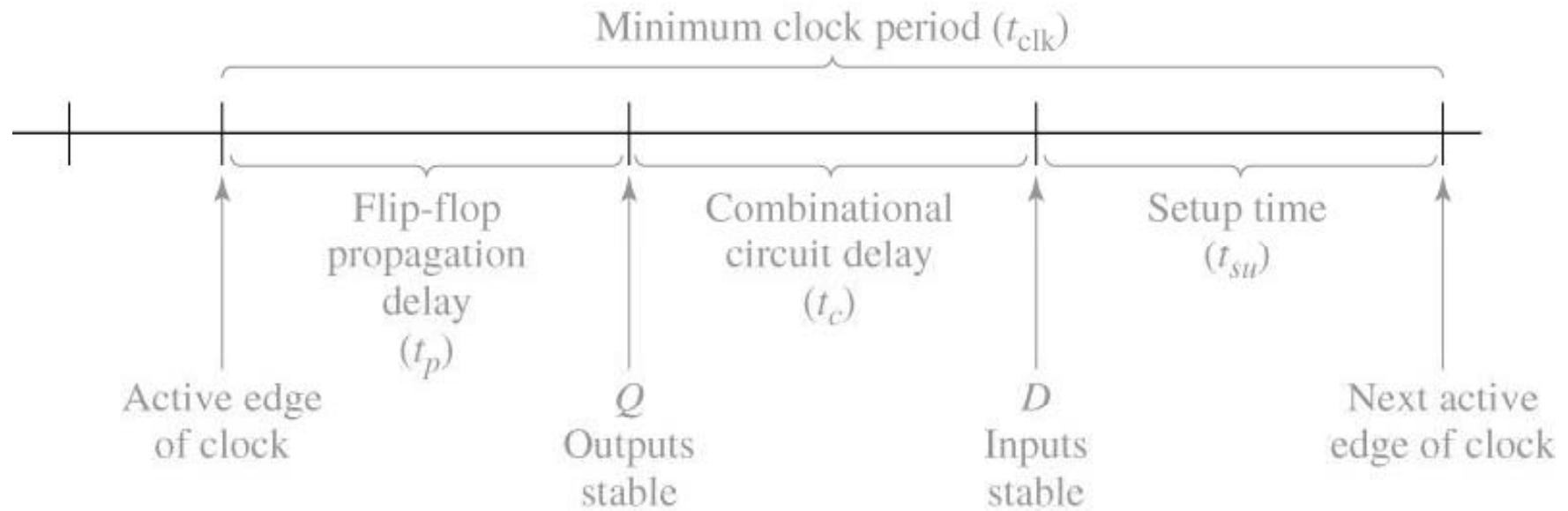


Figure 13-18: Minimum Clock Period for a Sequential Circuit

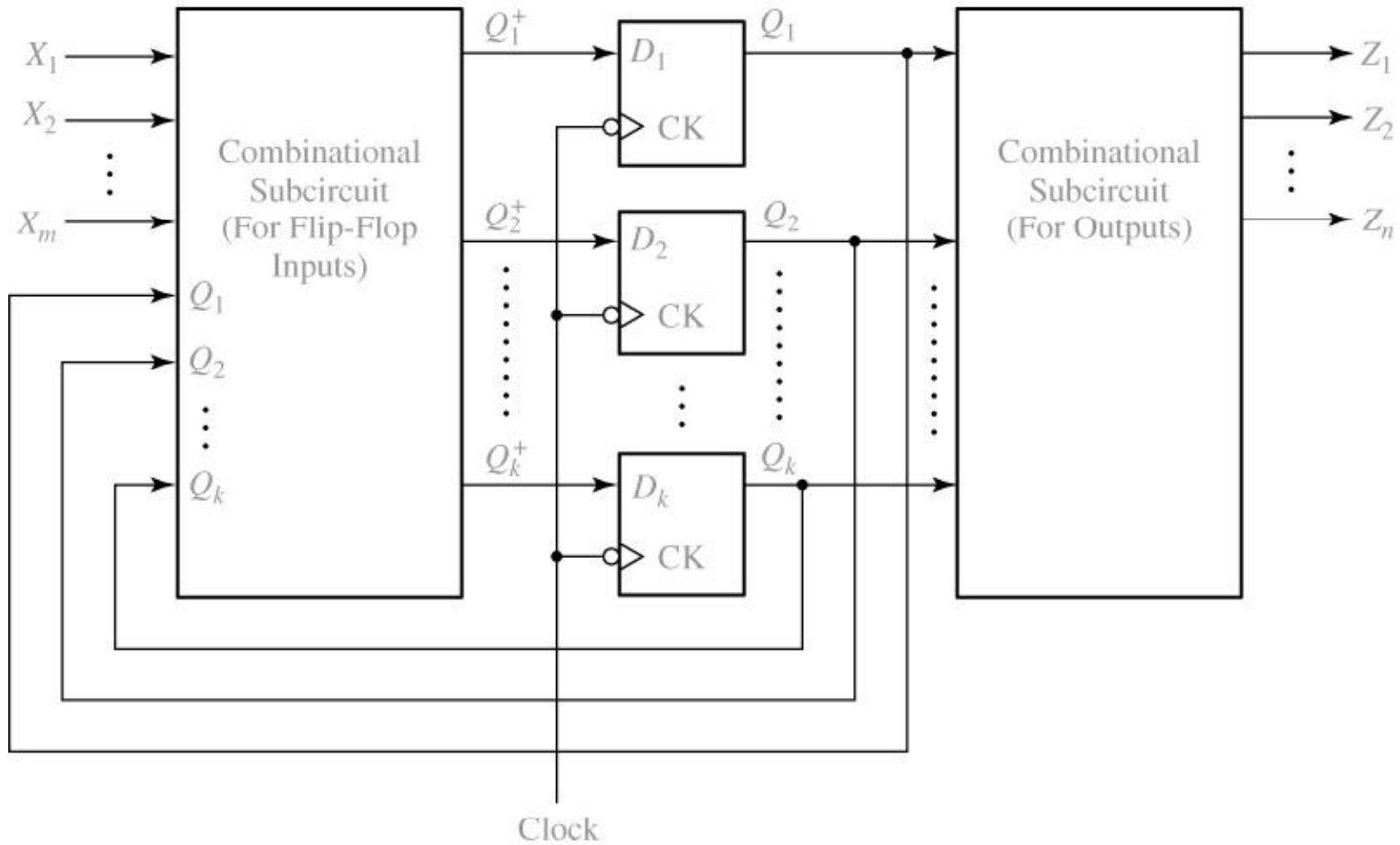
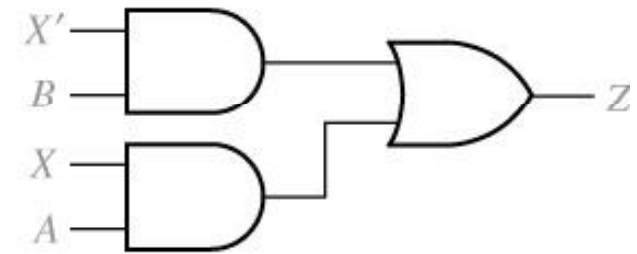
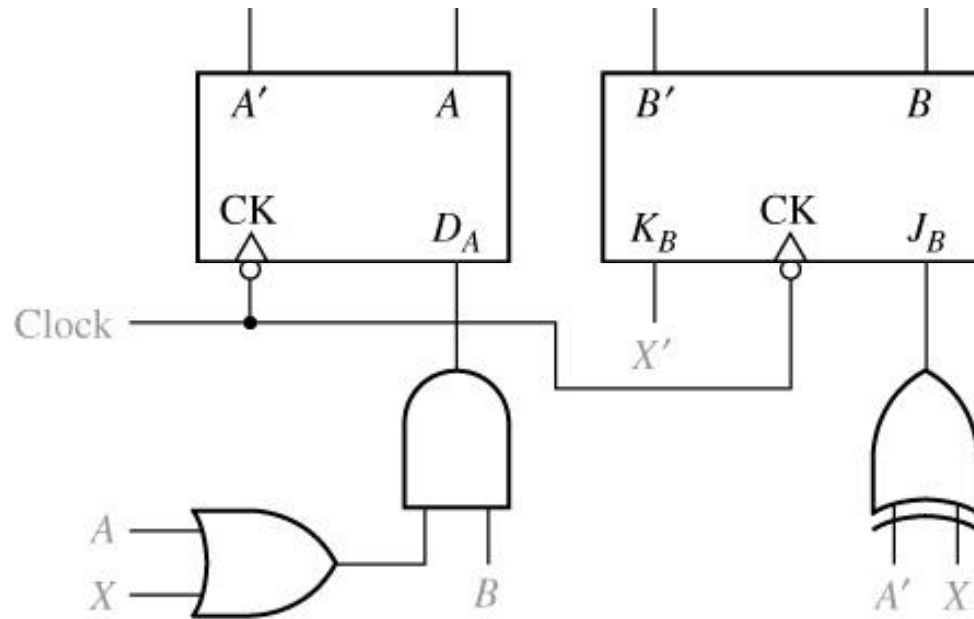


Figure 13-19: General Model for Moore Circuit Using Clocked D Flip-Flops



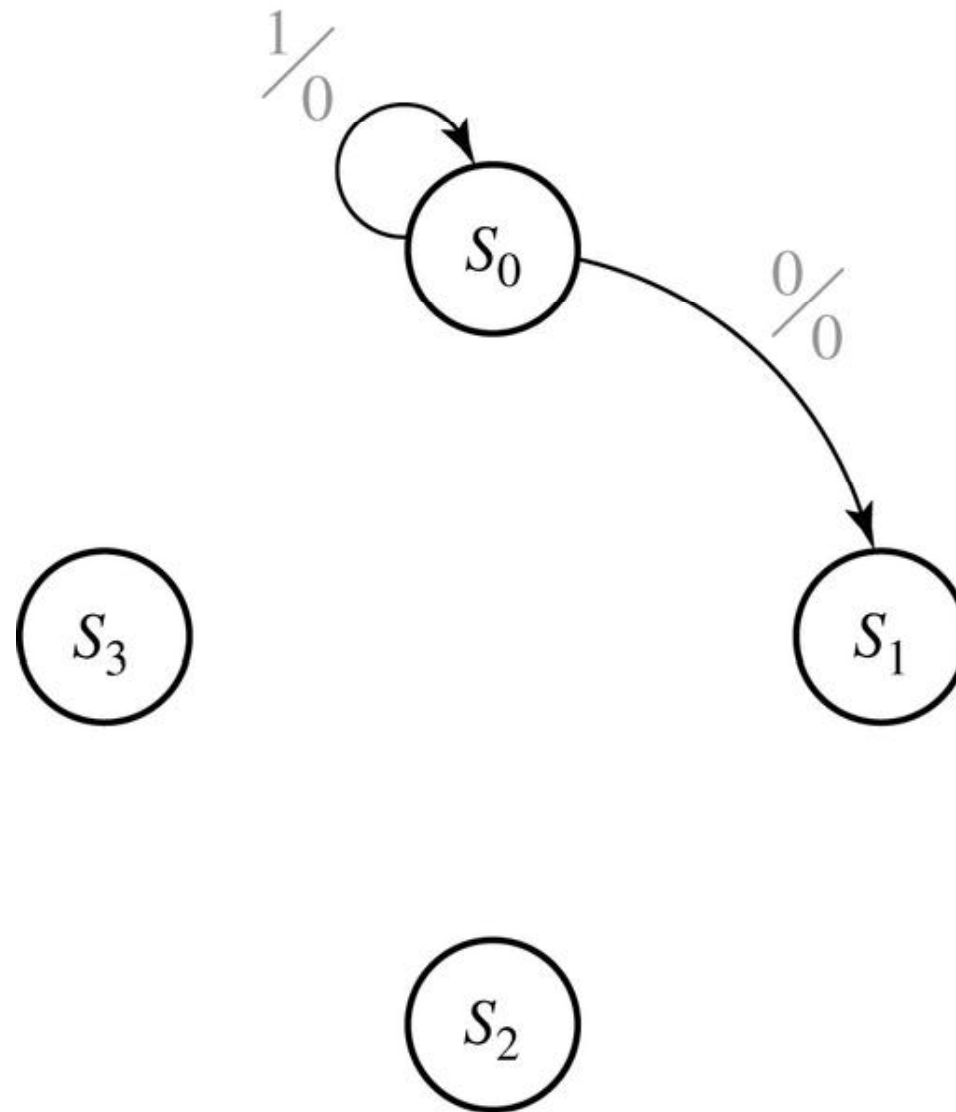
Programmed Exercise 13.1a

		X	
		0	1
AB			
00			
01			
11			
10			
		A^+	

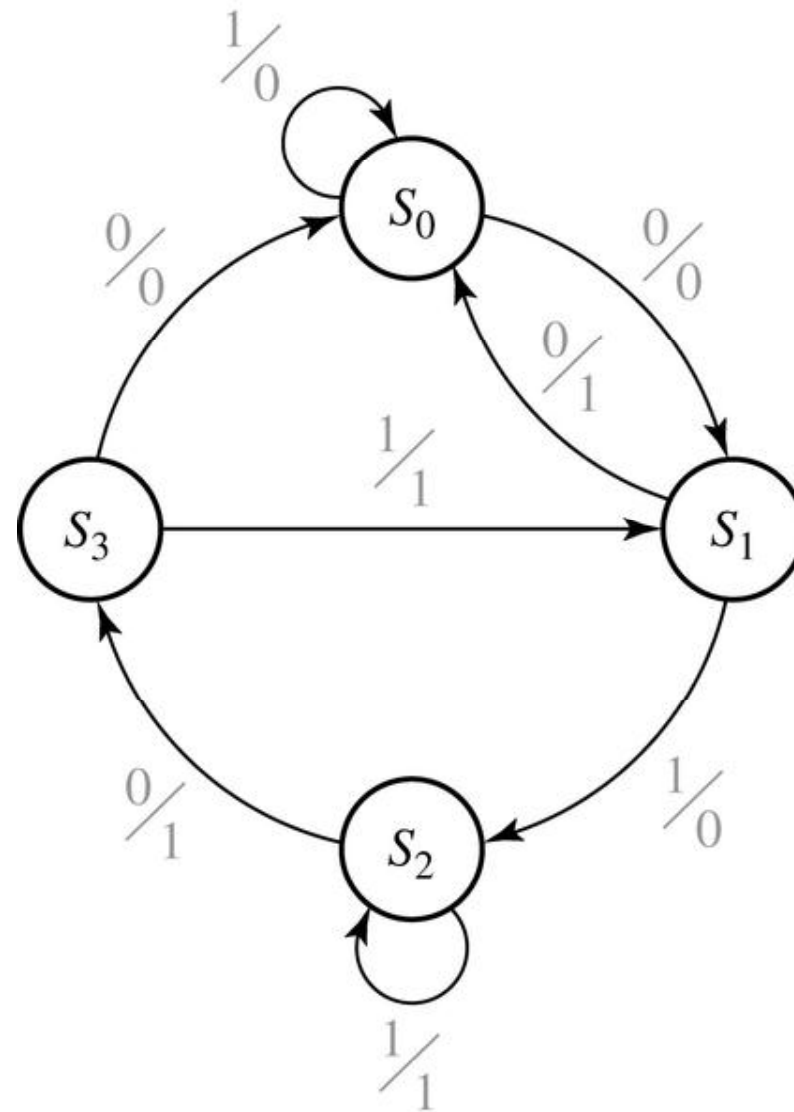
		X	
		0	1
AB			
00			
01			
11			
10			
		B^+	

		X	
		0	1
AB			
00			
01			
11			
10			
		Z	

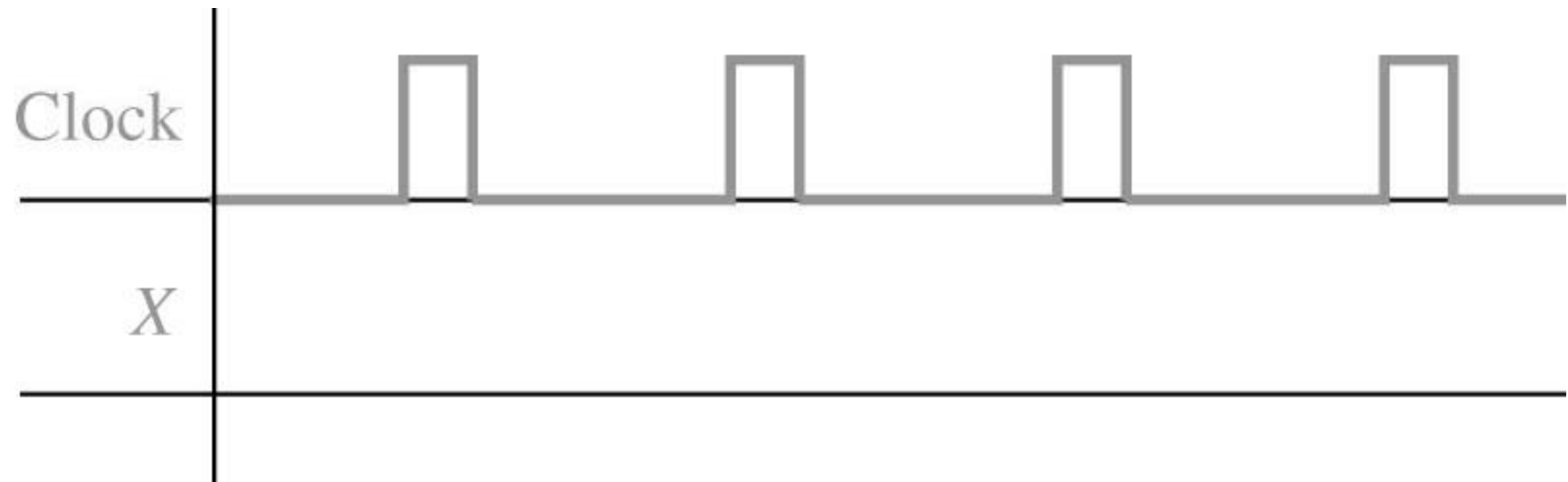
Programmed Exercise 13.1b



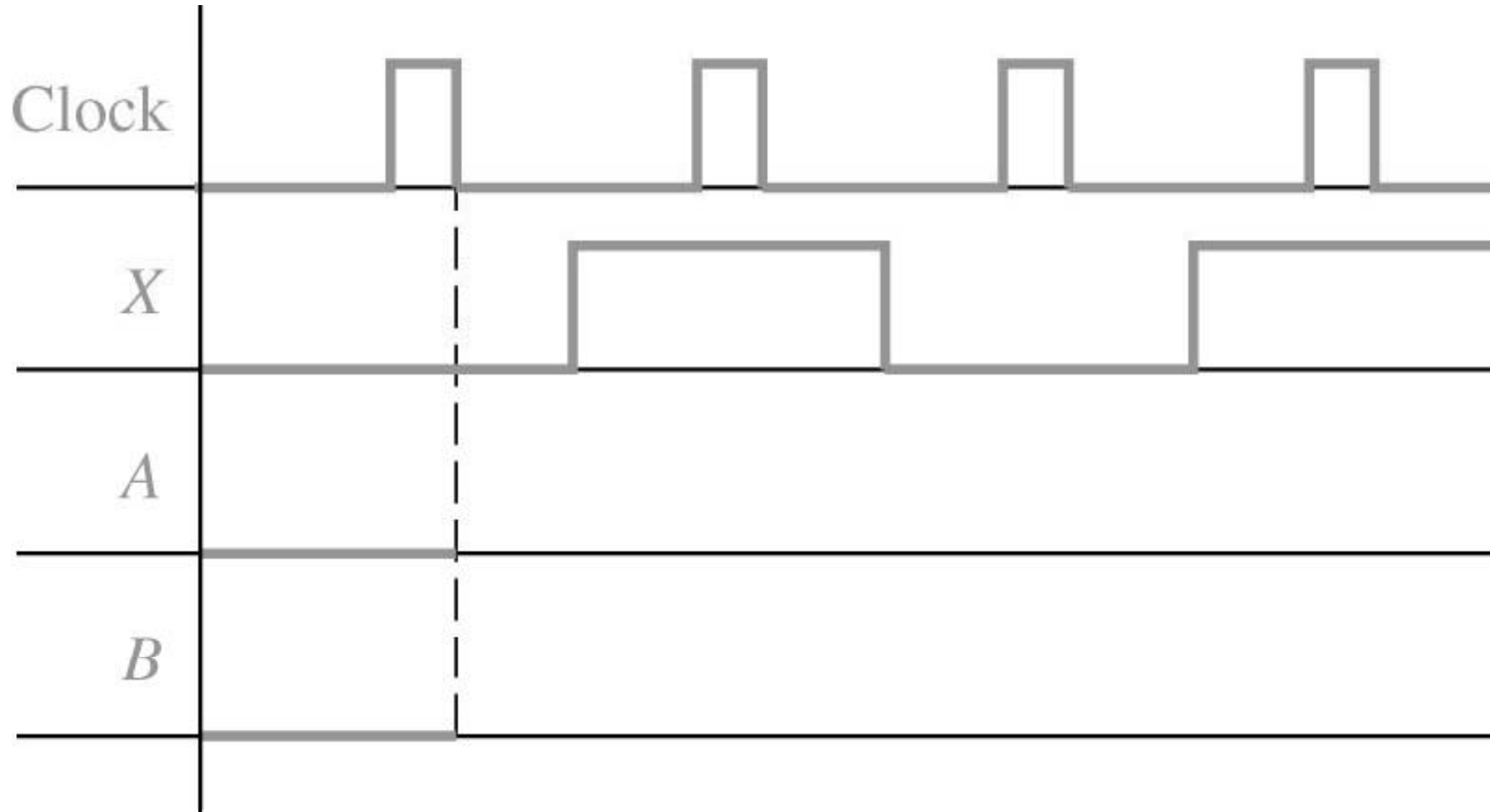
Programmed Exercise 13.1d



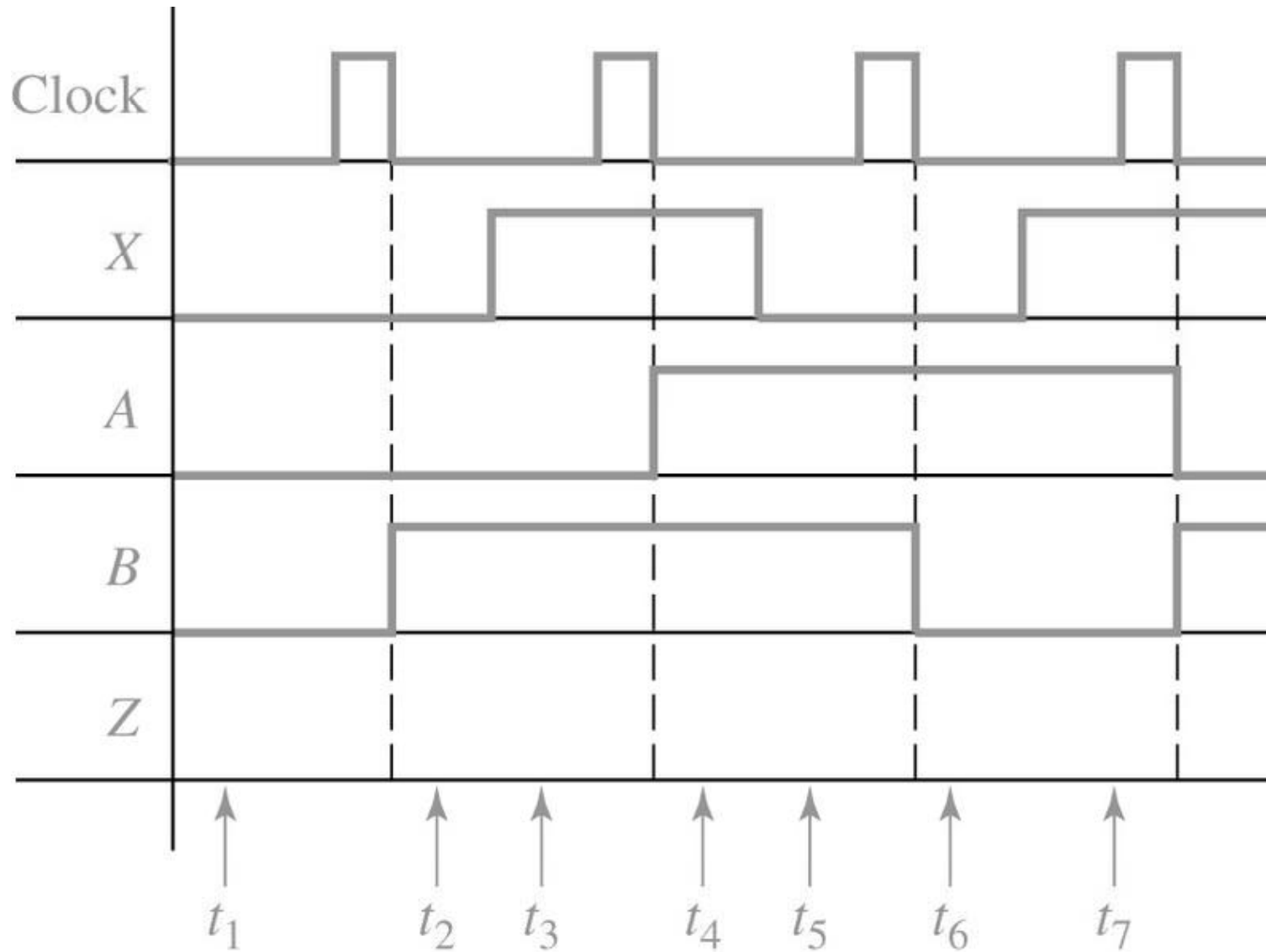
Programmed Exercise 13.1d (answer)



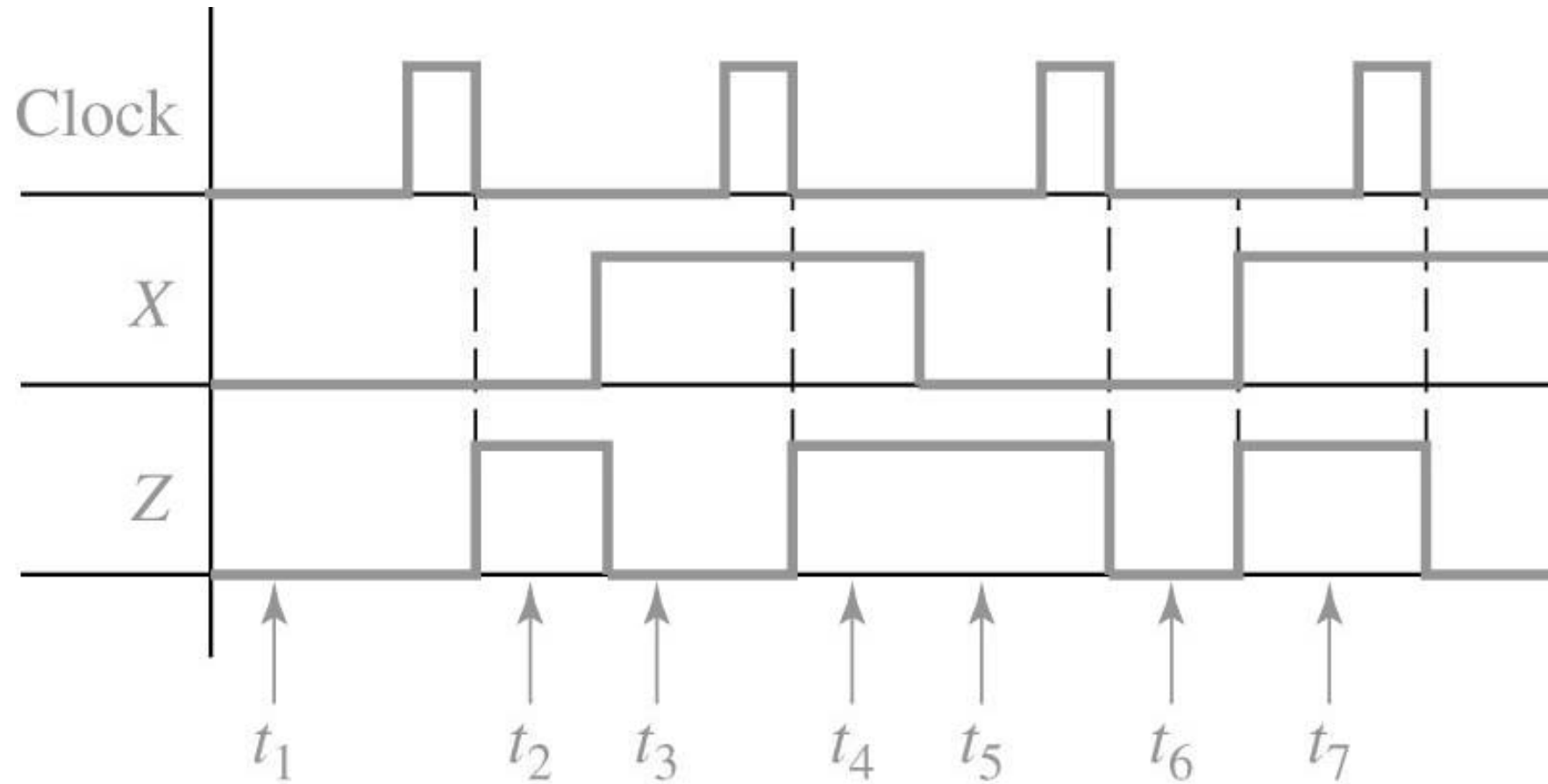
Programmed Exercise 13.1f



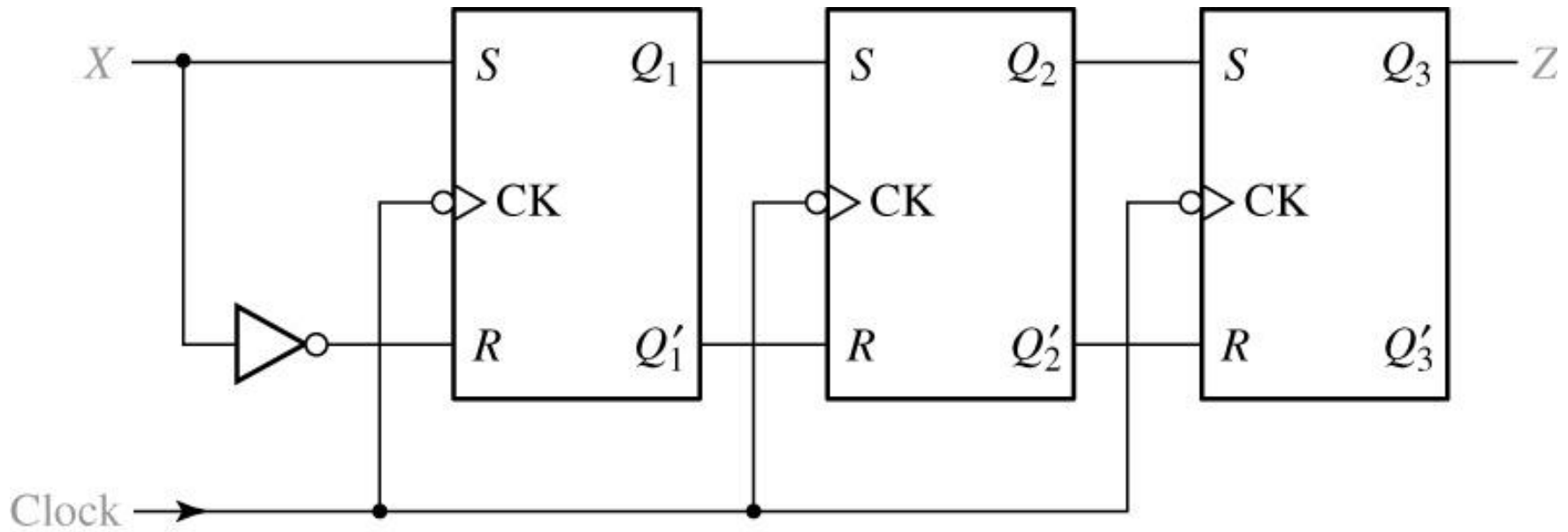
Programmed Exercise 13.1f (answer)



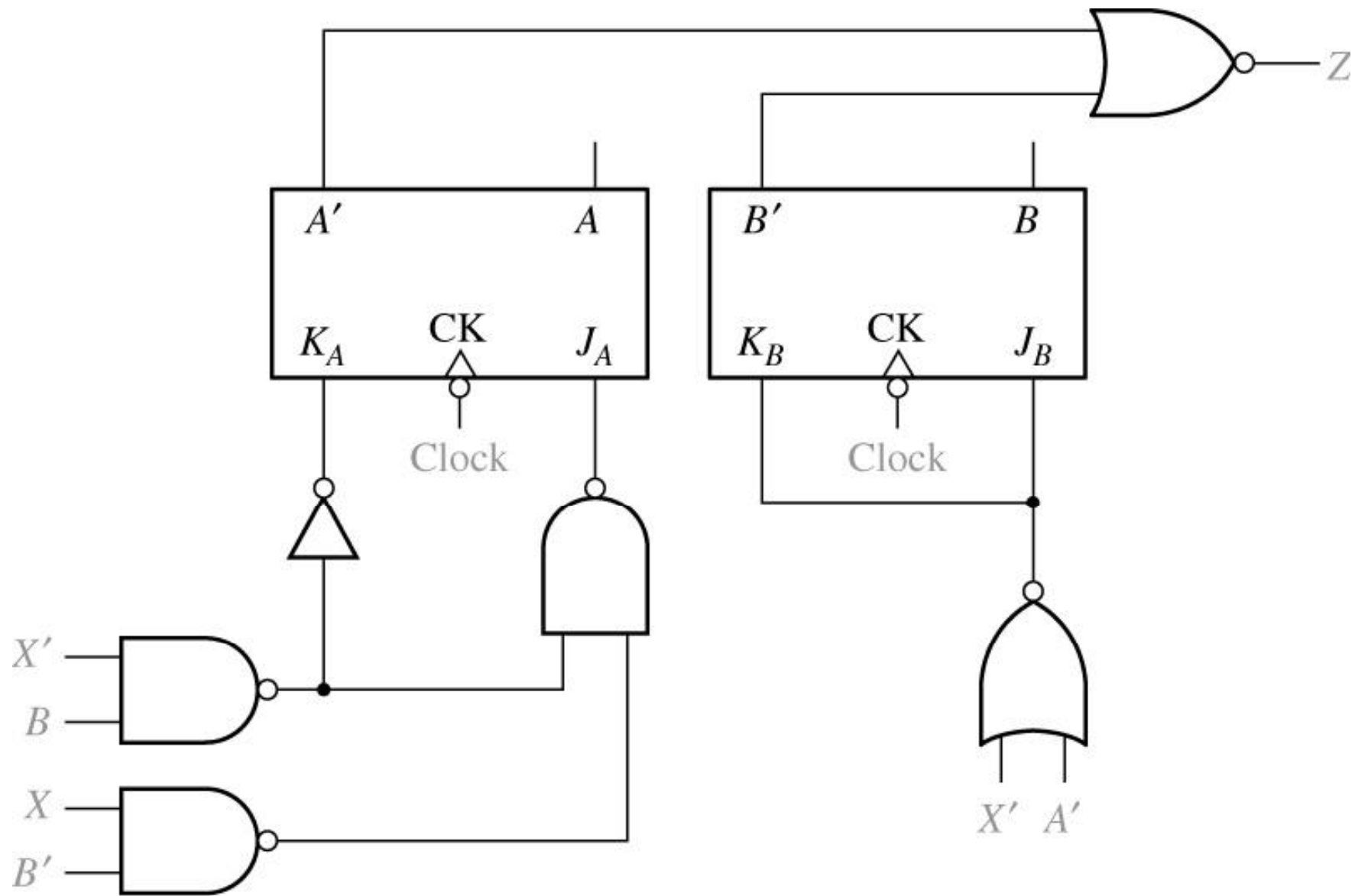
Programmed Exercise 13.1g (answer)



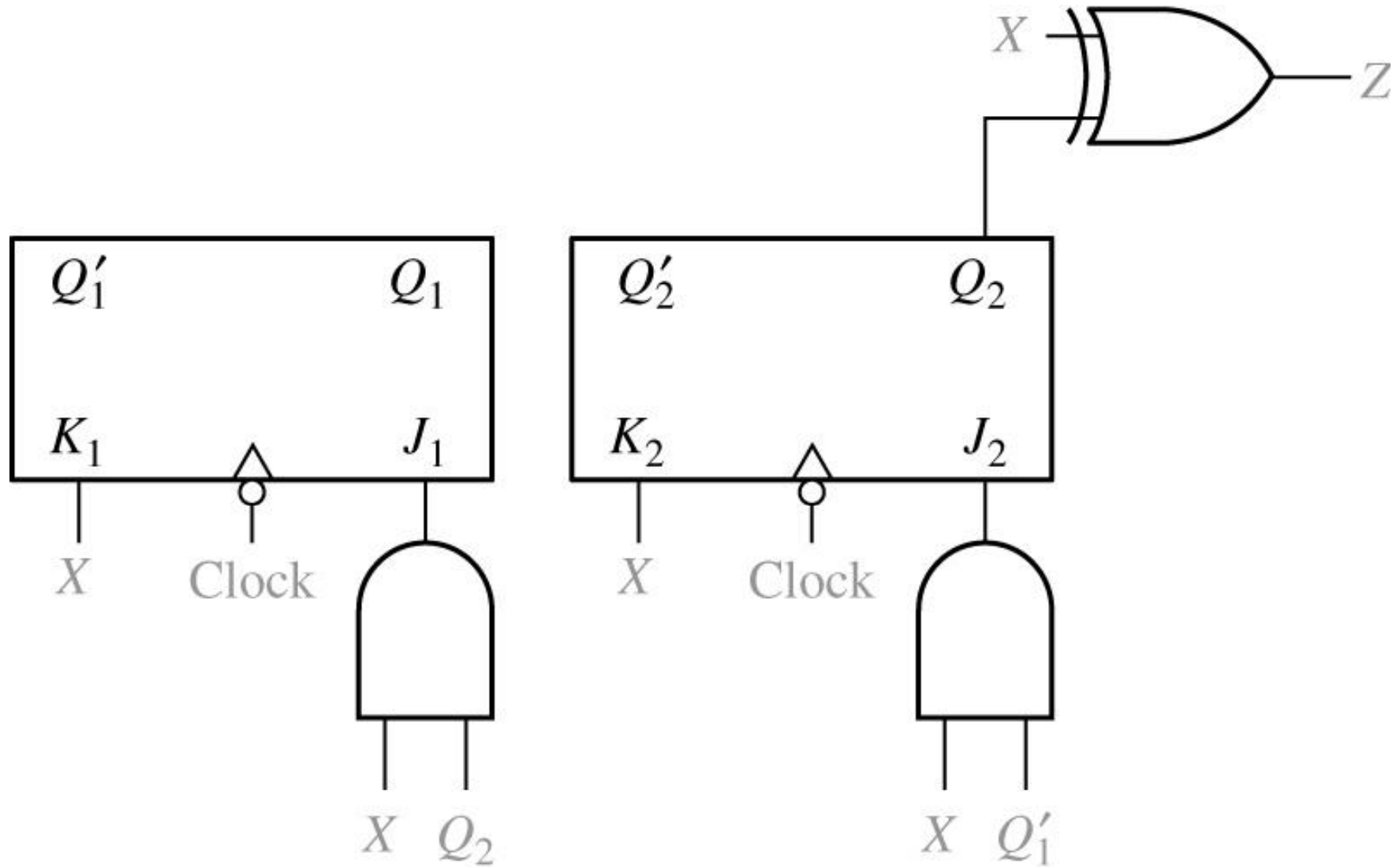
Programmed Exercise 13.1h (answer)



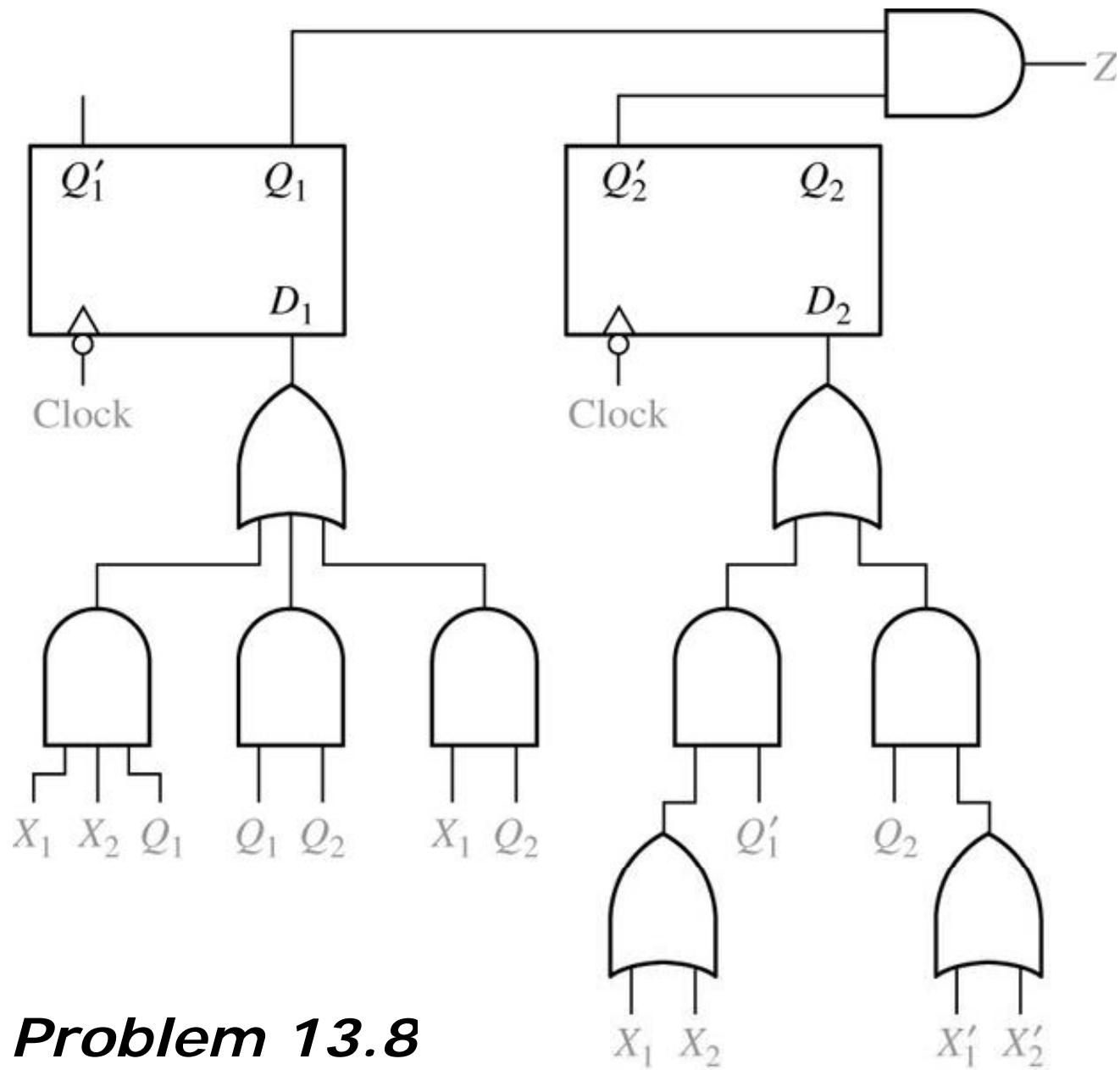
Problem 13.2



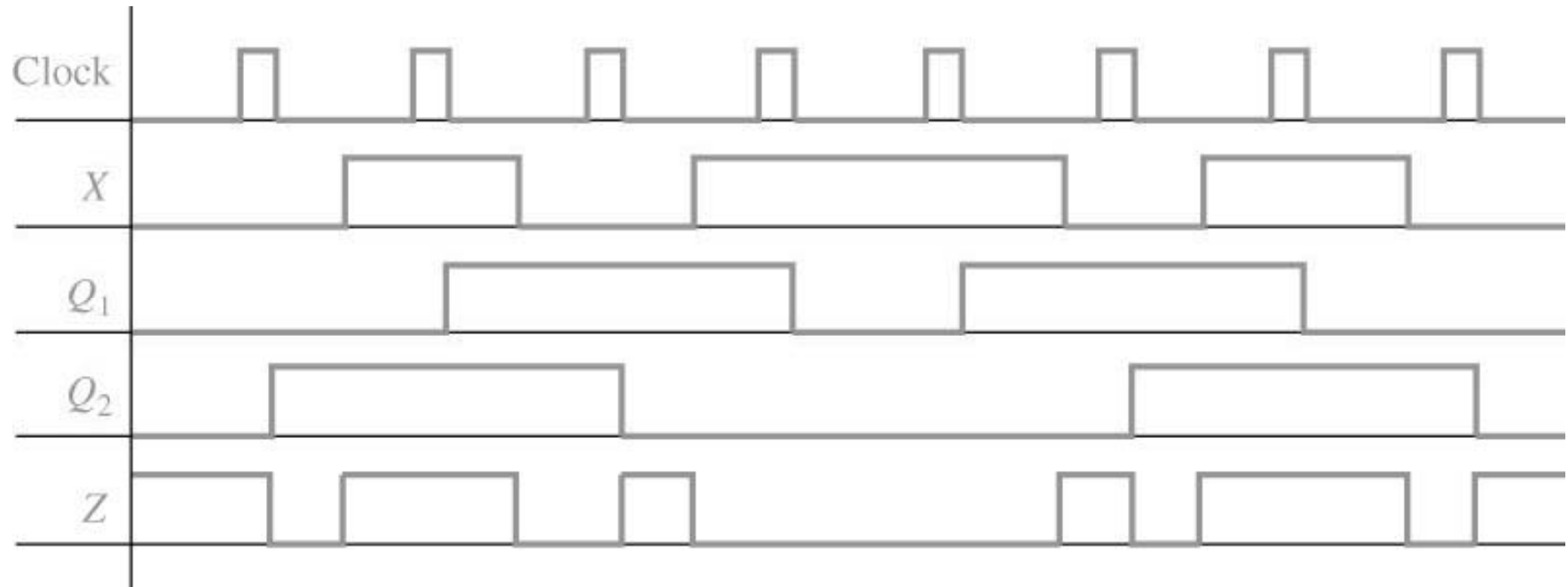
Problem 13.3



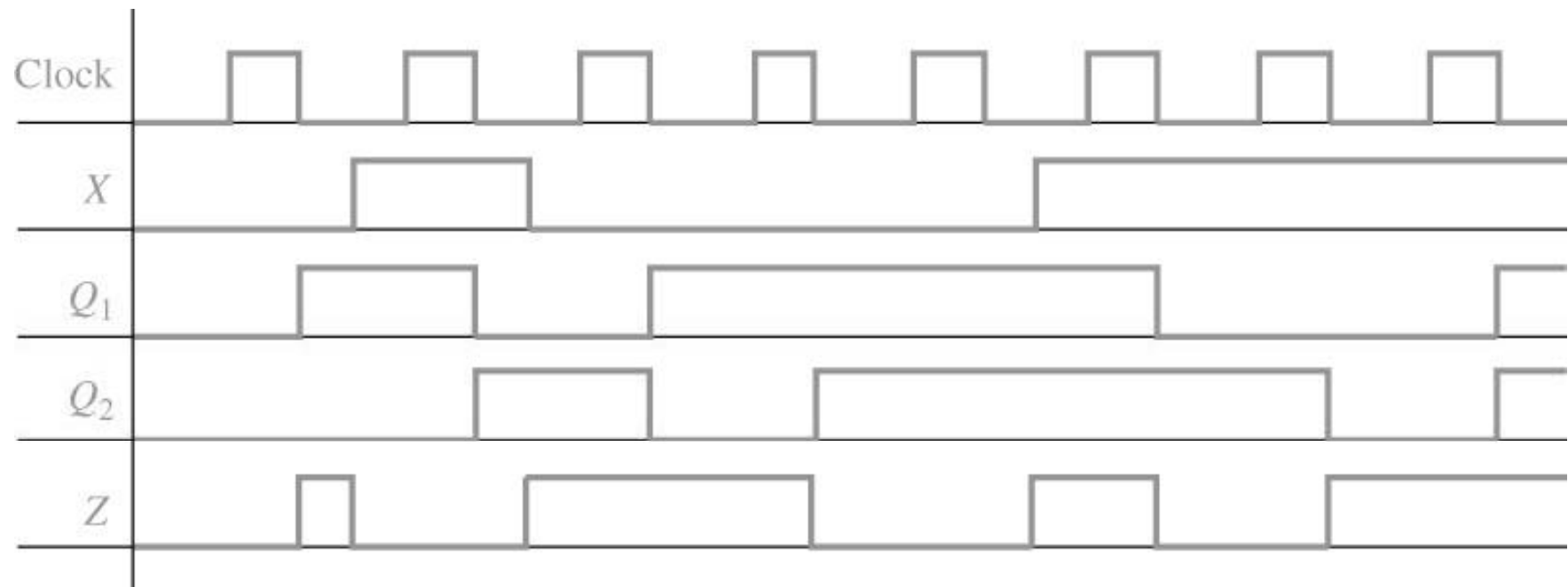
Problem 13.7



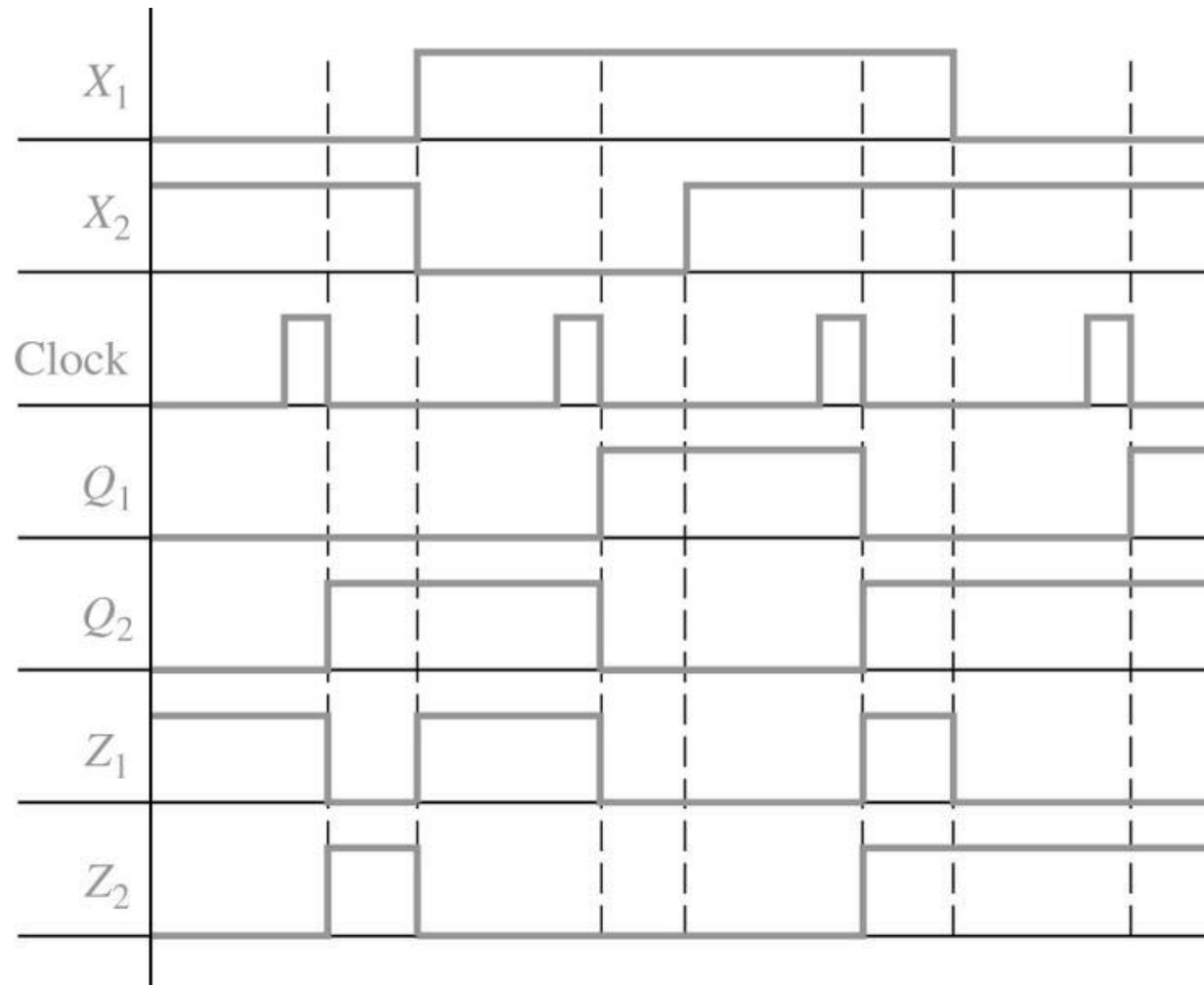
Problem 13.8



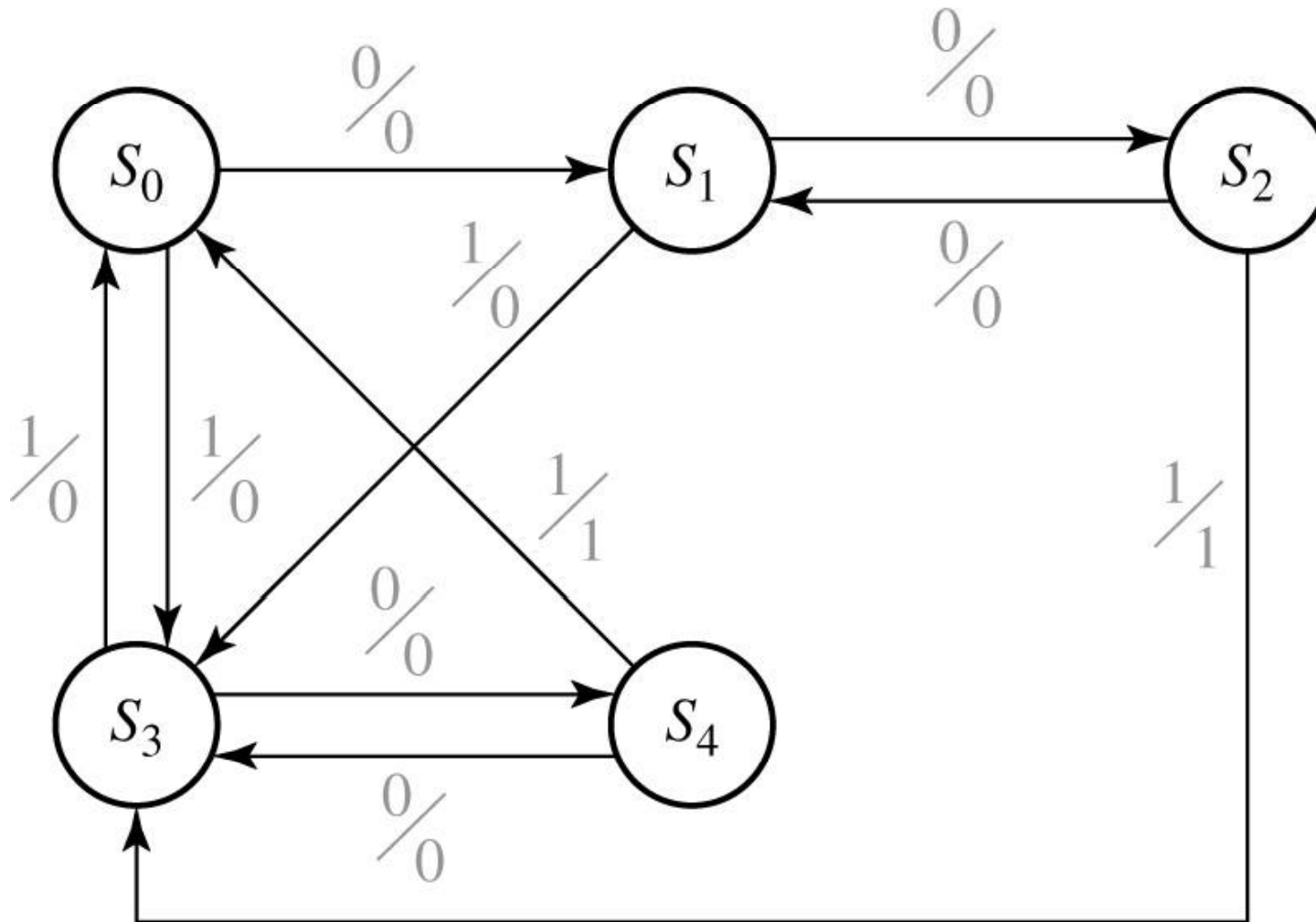
Problem 13.13



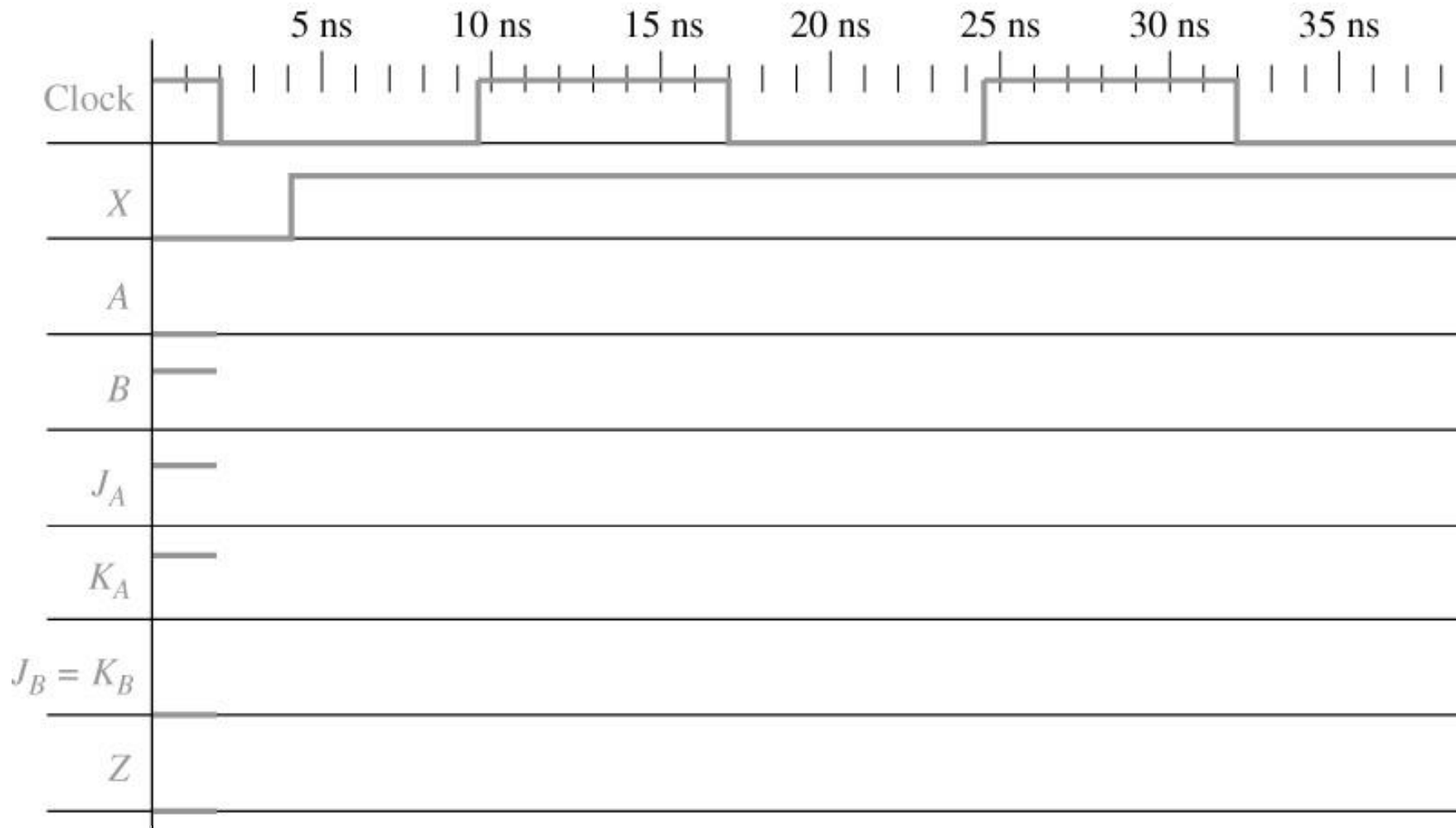
Problem 13.14



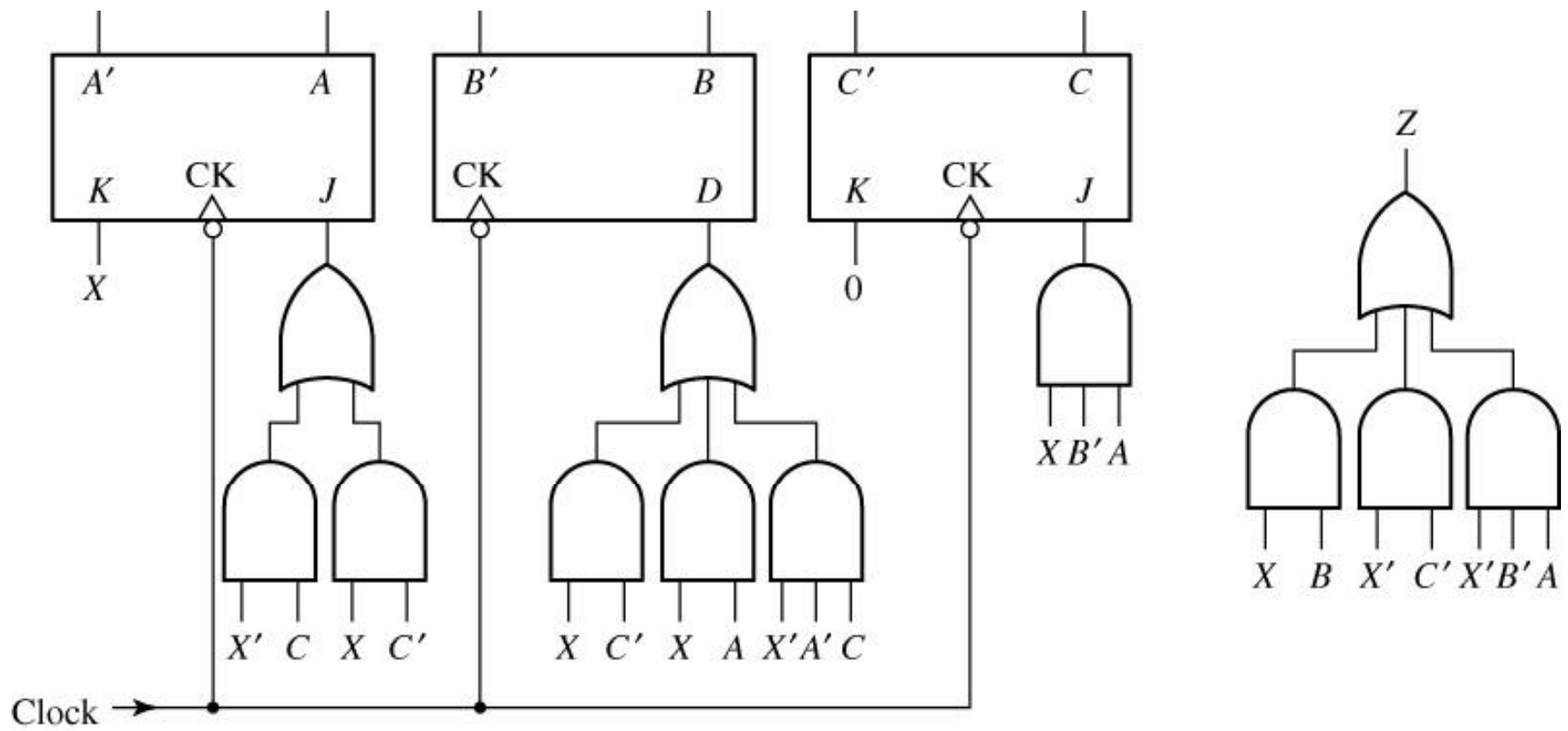
Problem 13.15



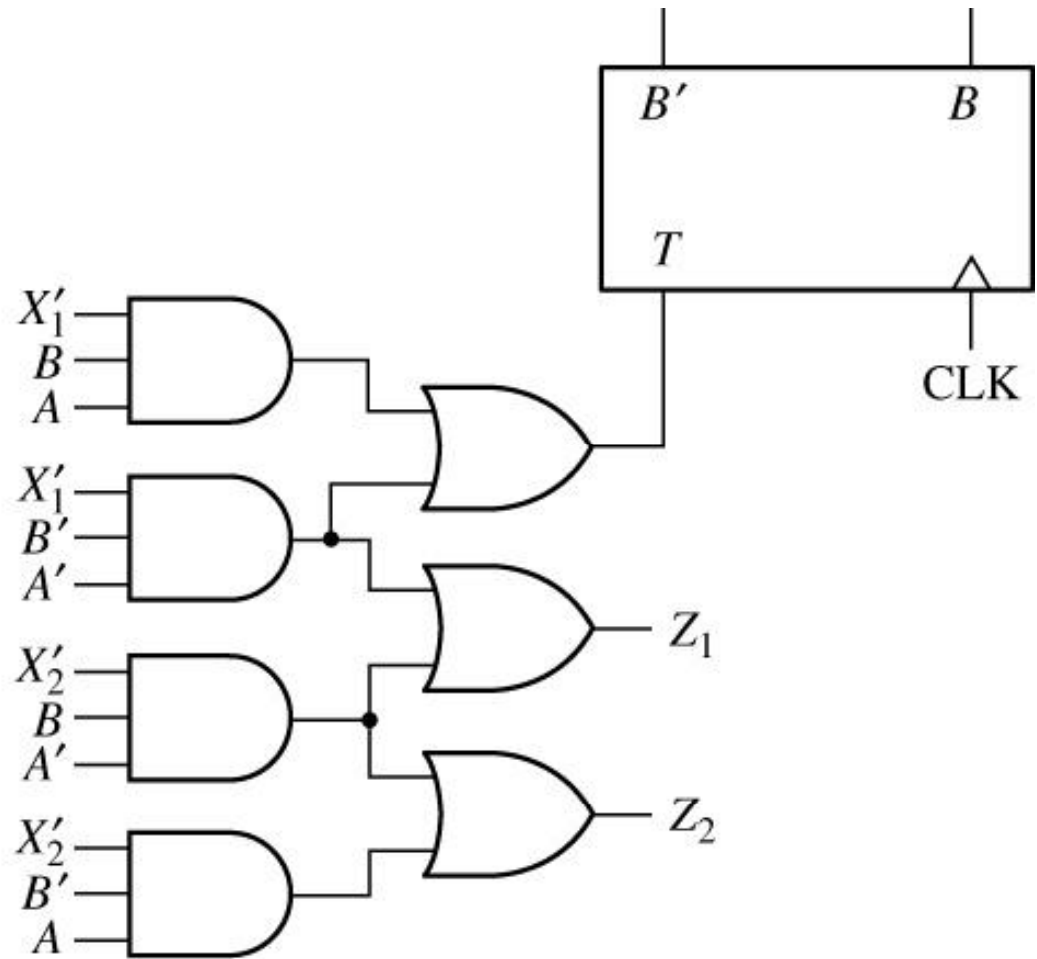
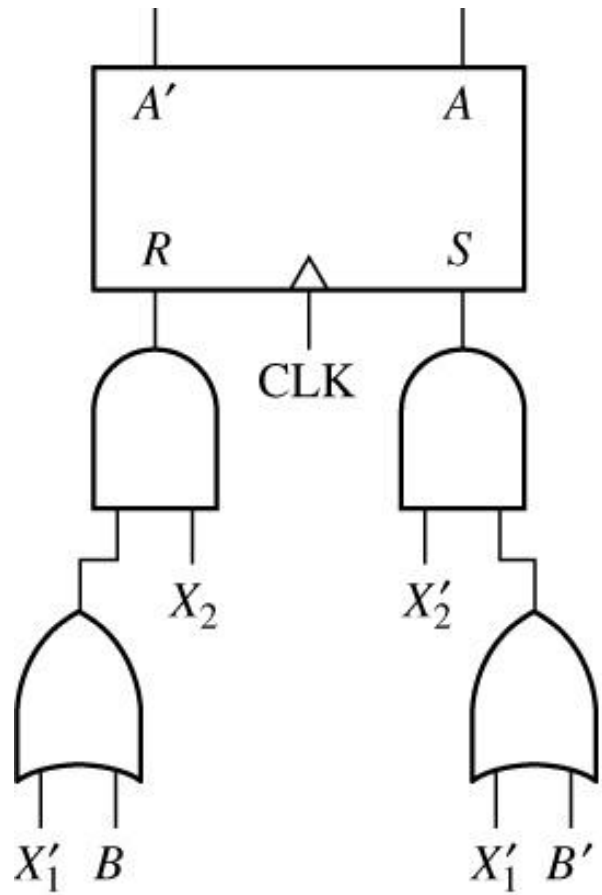
Problem 13.17



Problem 13.18



Problem 13.19



Problem 13.20