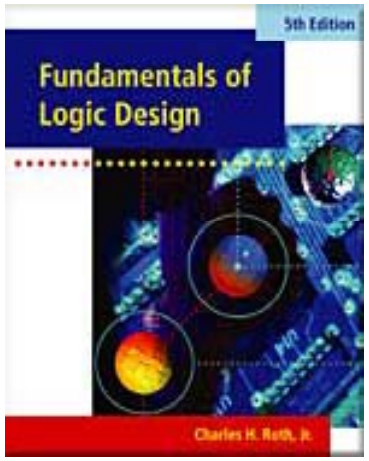
FIGURES FOR

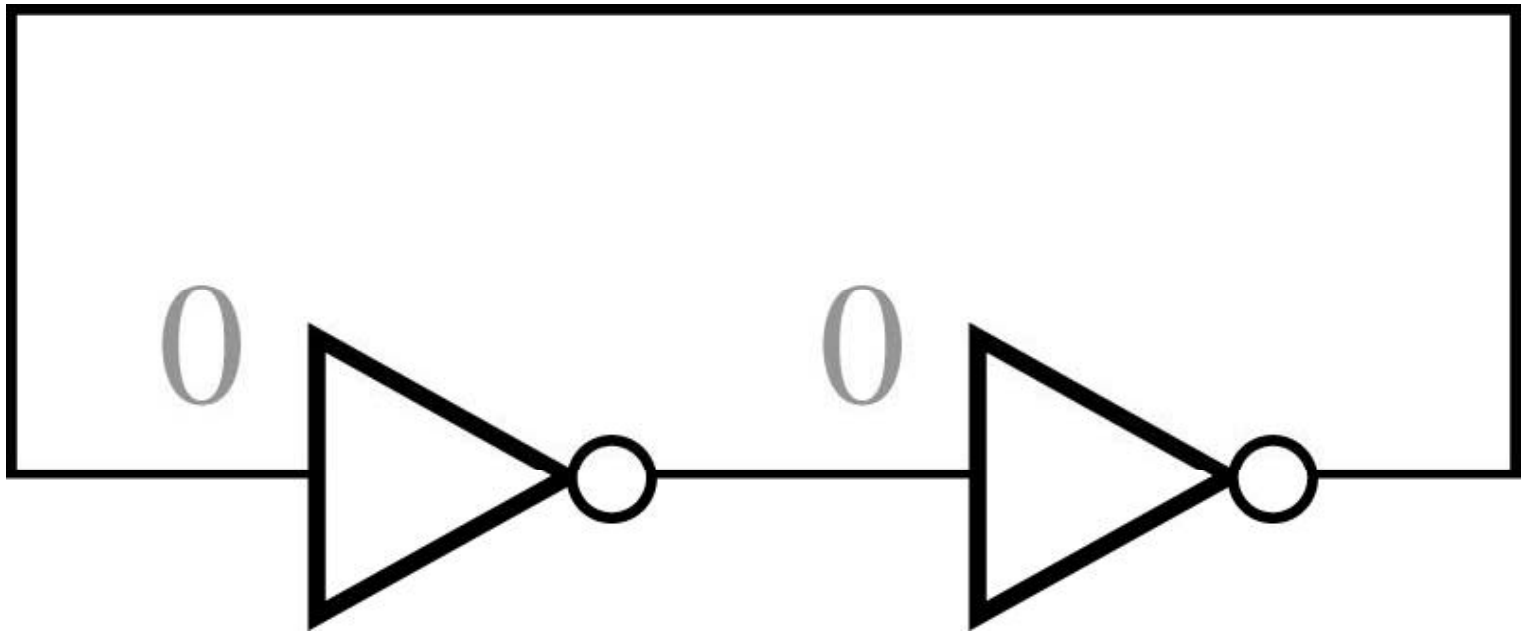
CHAPTER 11

LATCHES AND FLIP-FLOPS

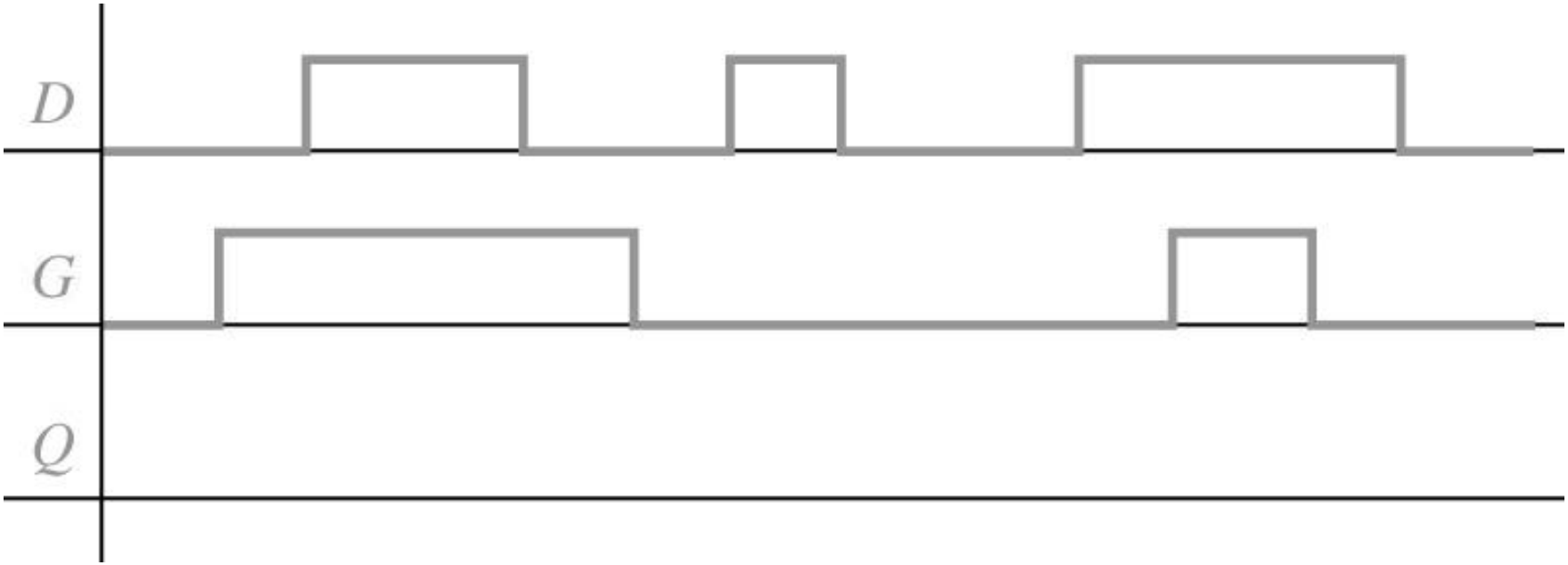


This chapter in the book includes:

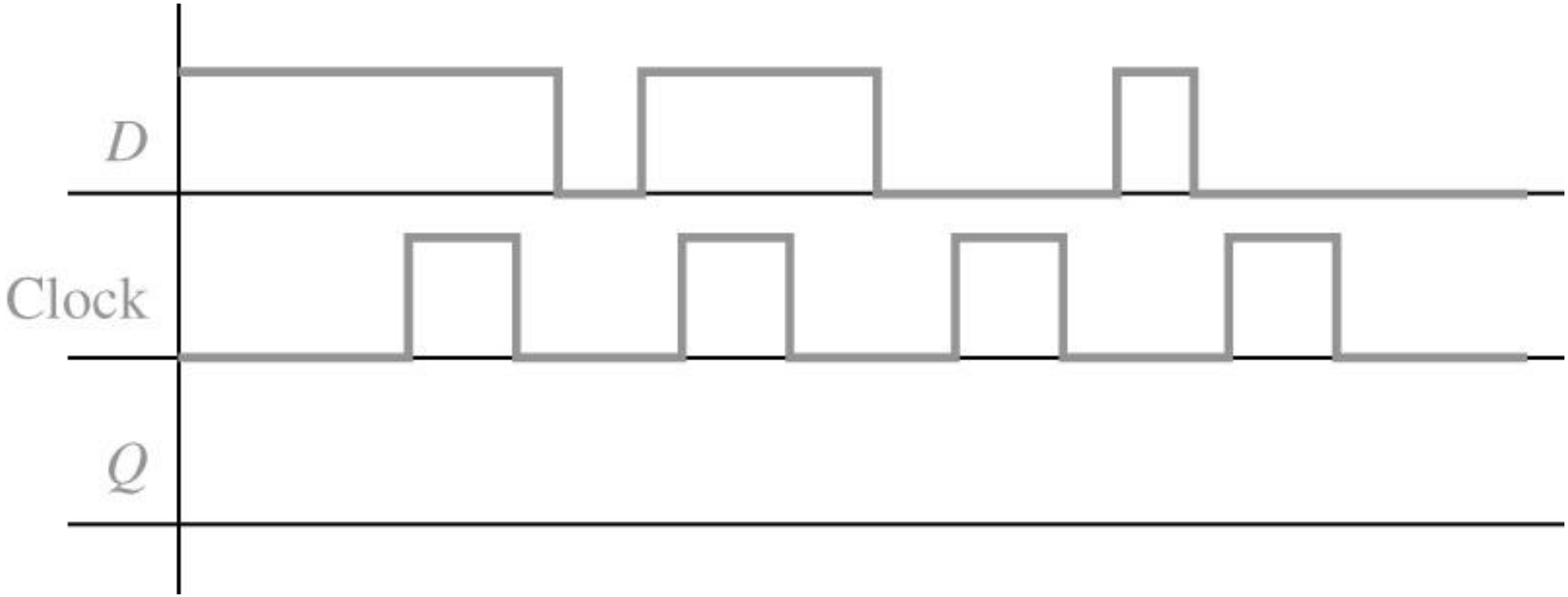
Click the mouse to move to the next page.
Use the ESC key to exit this chapter.



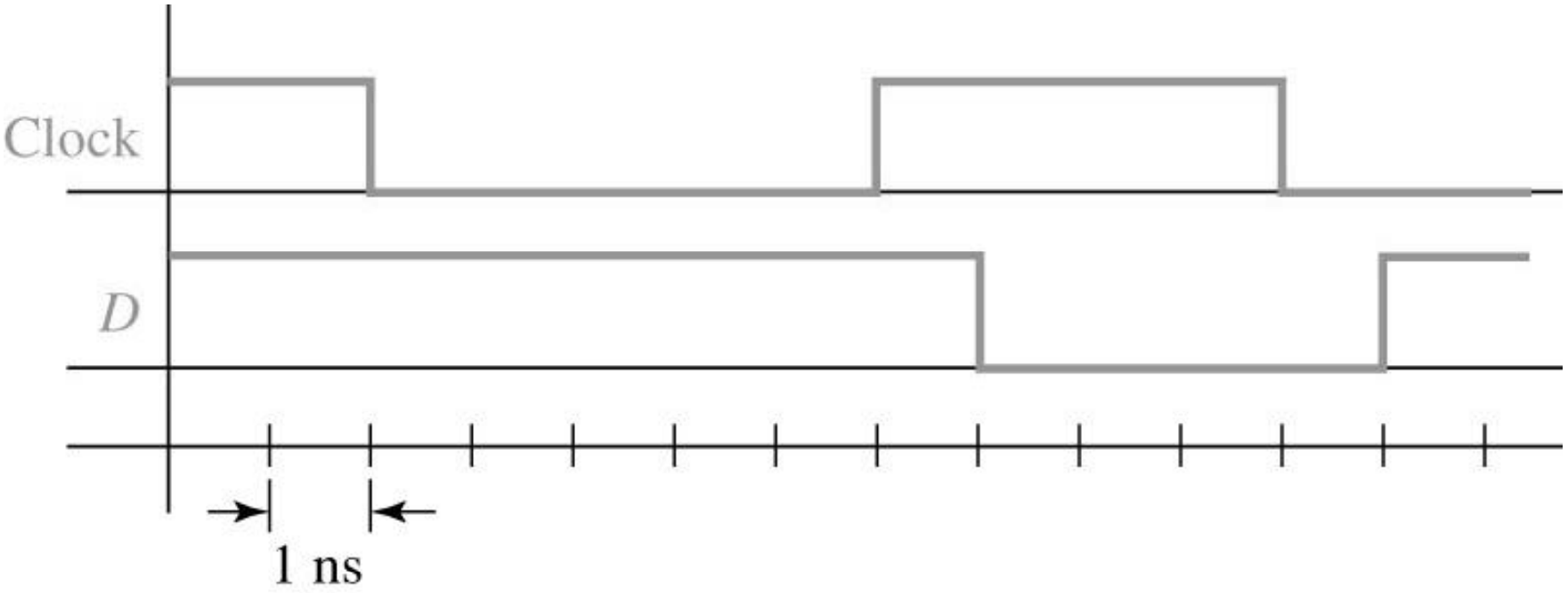
Study Guide, No. 1



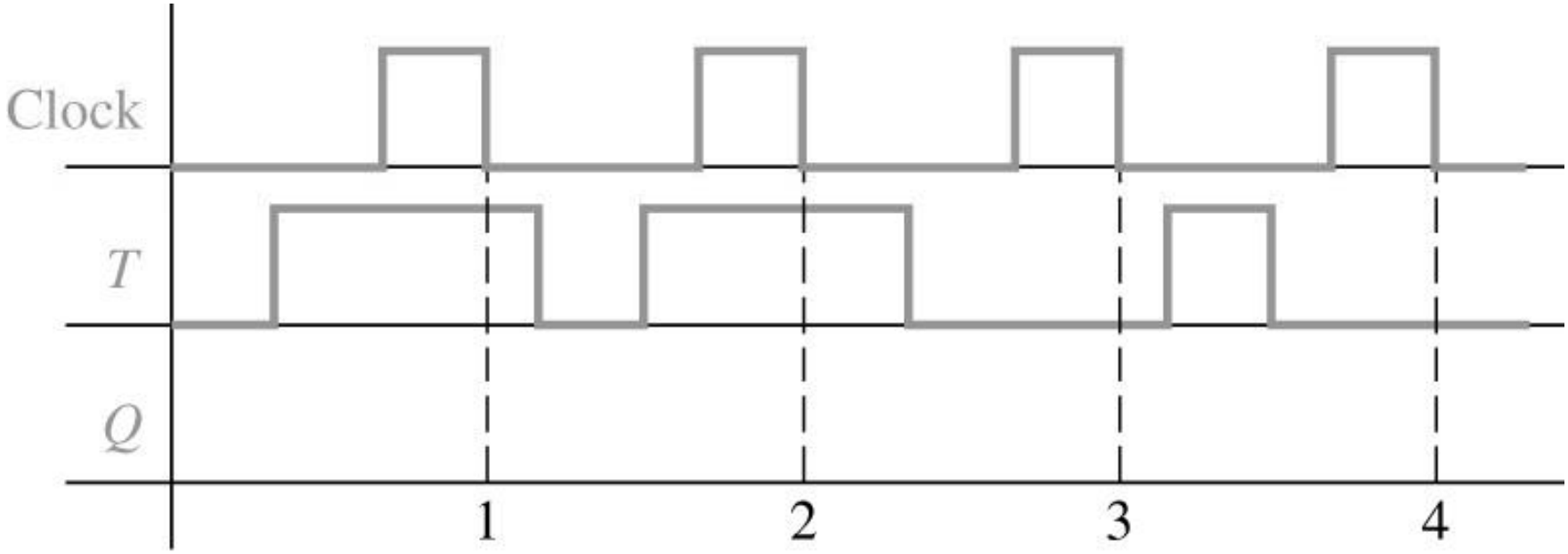
Study Guide, No. 3c



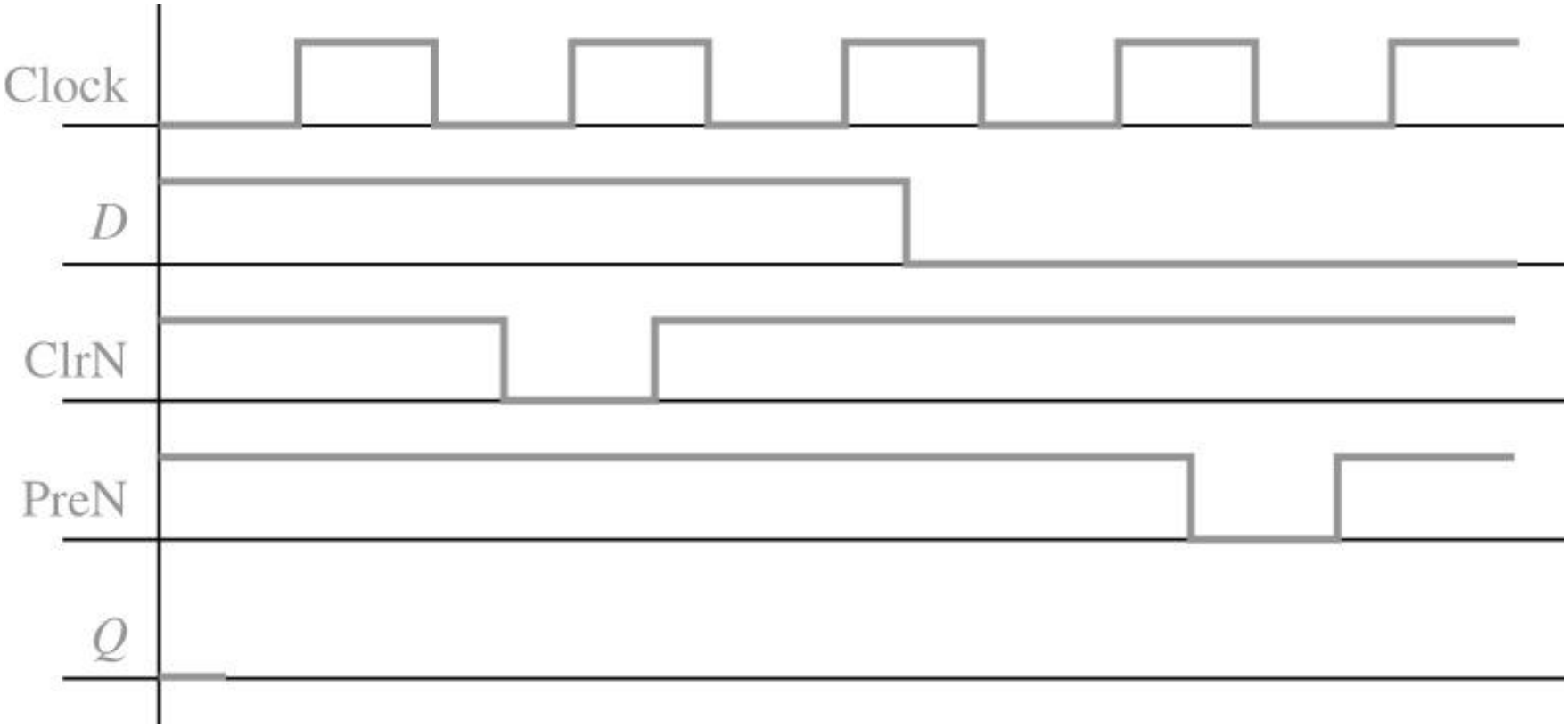
Study Guide, No. 4b



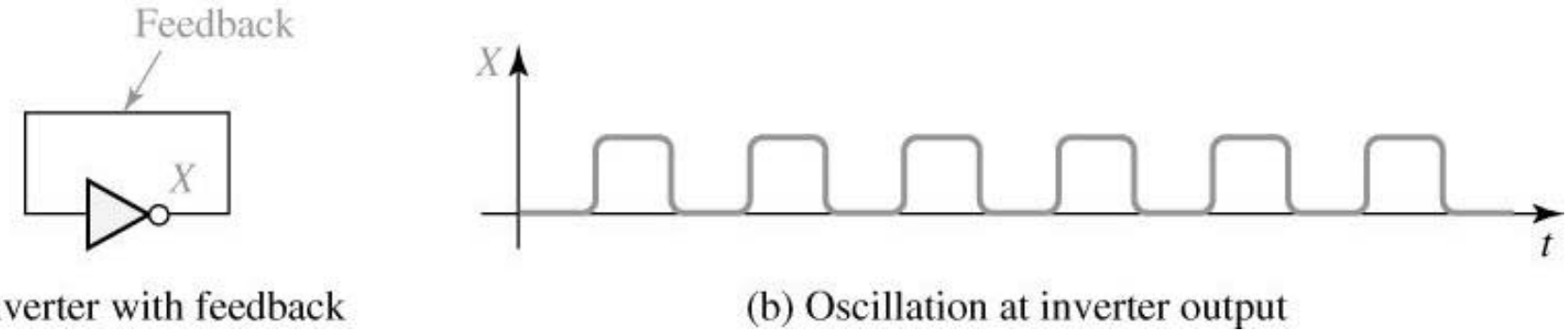
Study Guide, No. 4d



Study Guide, No. 7b



Study Guide, No. 8b



(a) Inverter with feedback

(b) Oscillation at inverter output

Figure 11-1

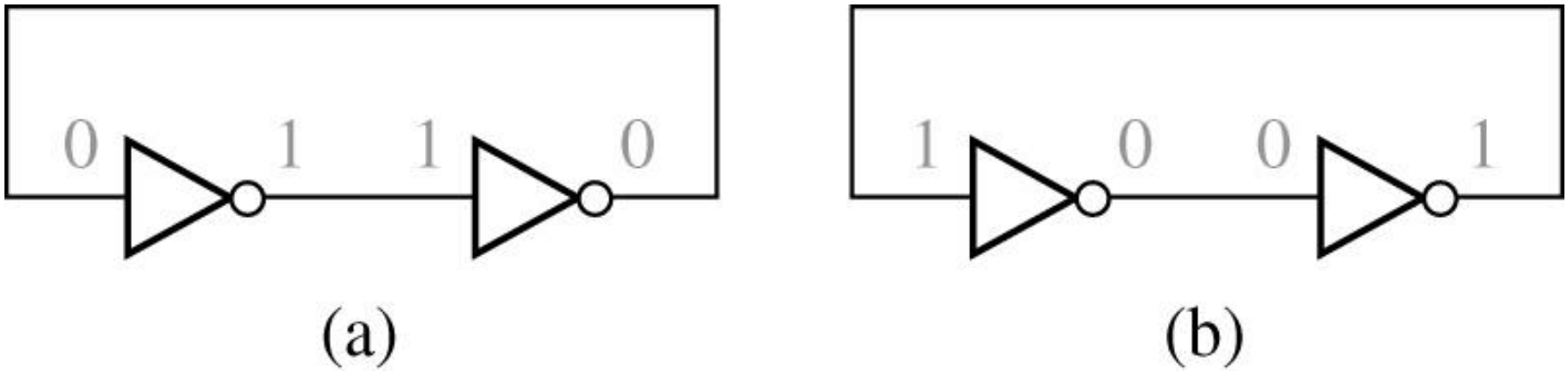


Figure 11-2

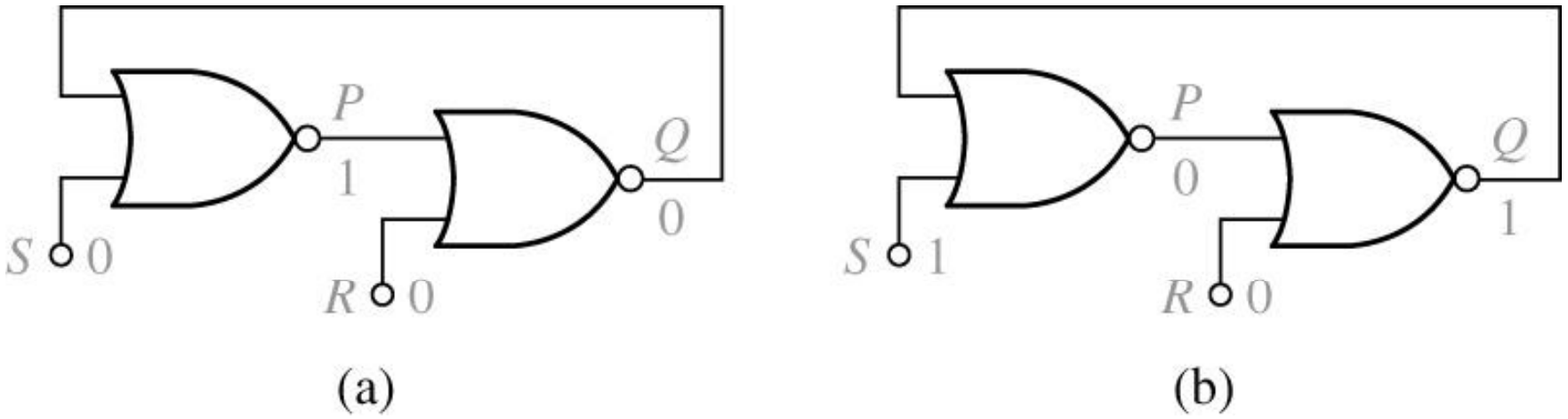


Figure 11-3

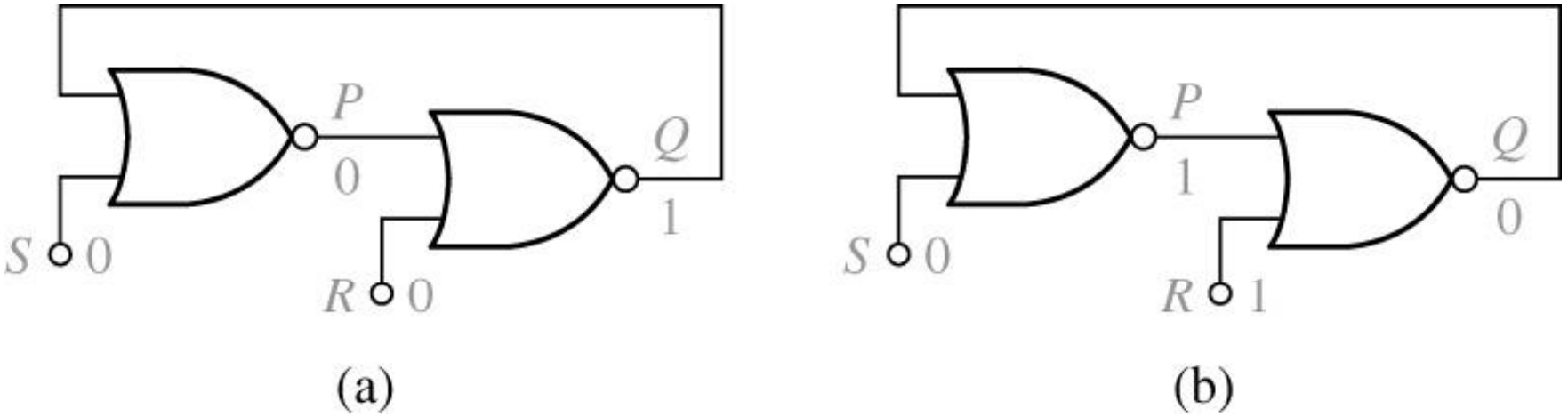


Figure 11-4

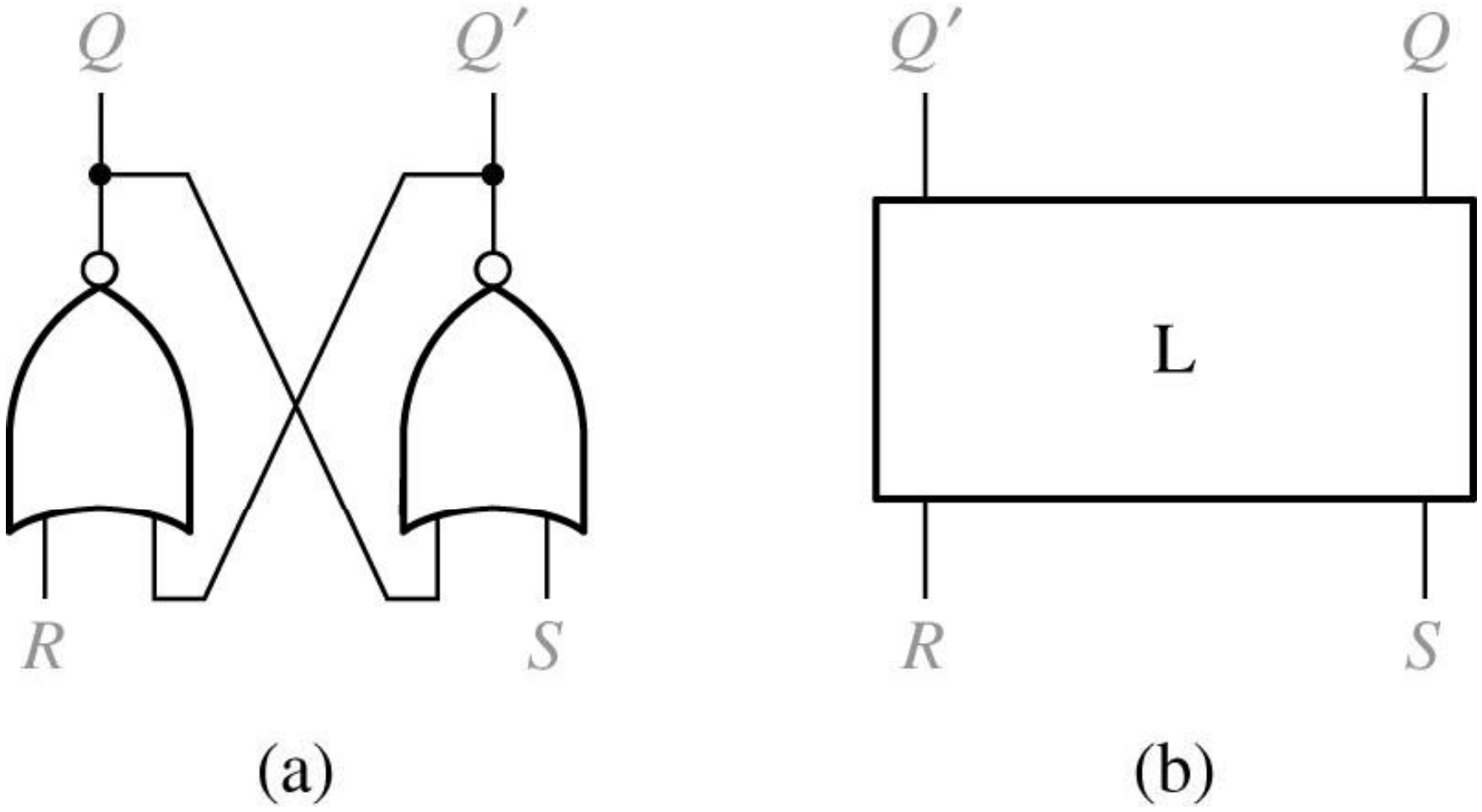


Figure 11-5: **S-R Latch**

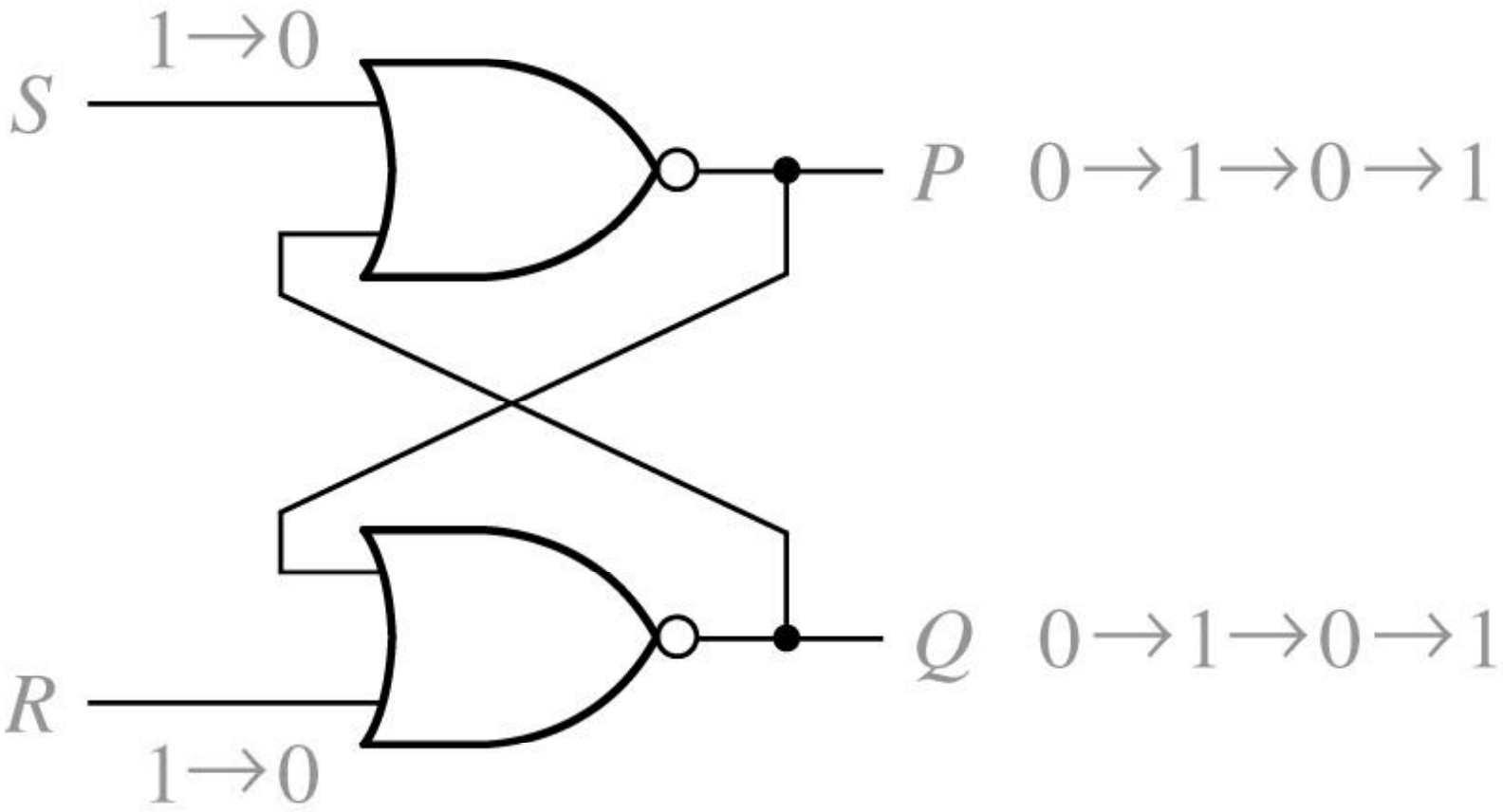


Figure 11-6: **Improper S-R Latch Operation**

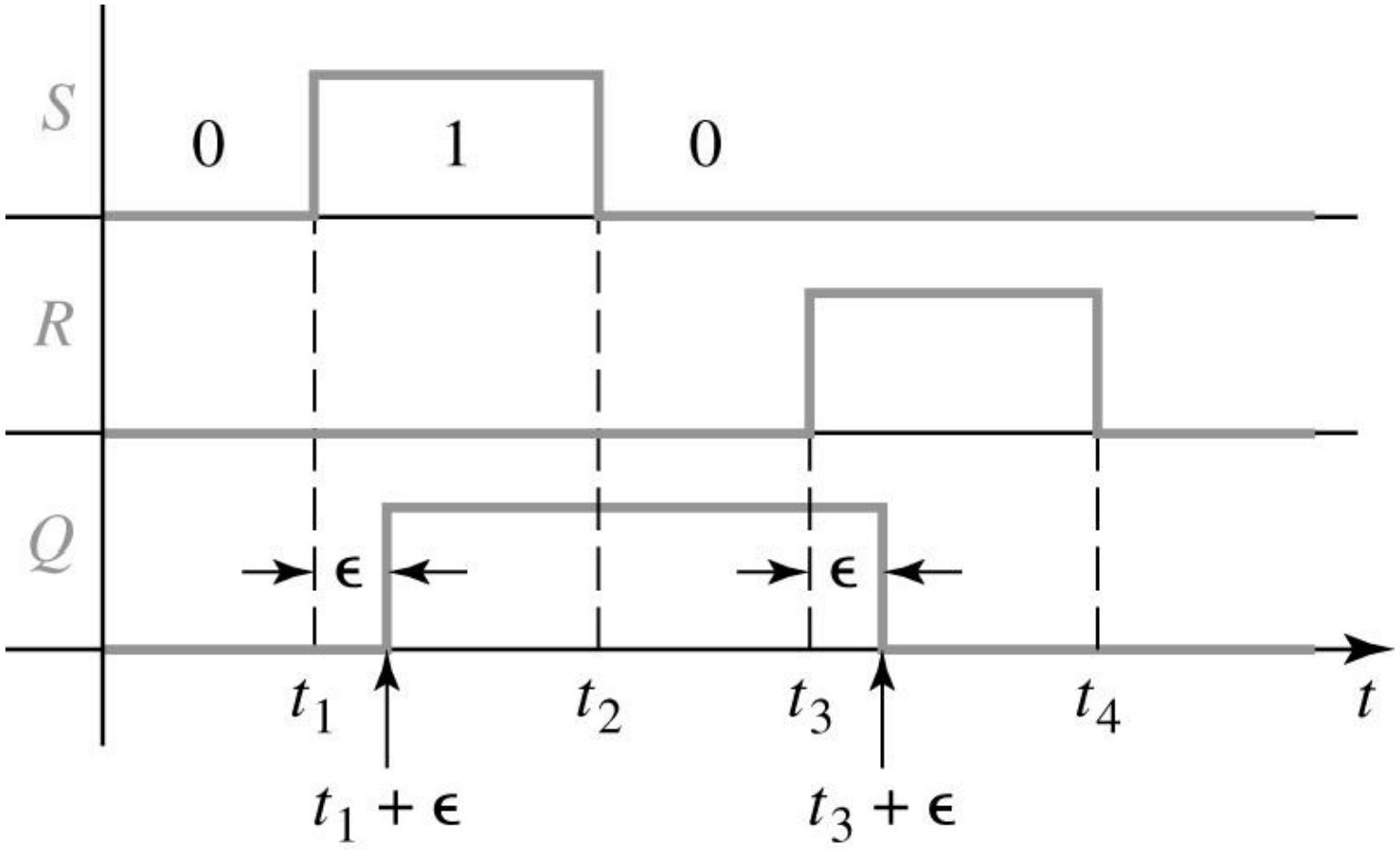


Figure 11-7: **Timing Diagram for S-R Latch**

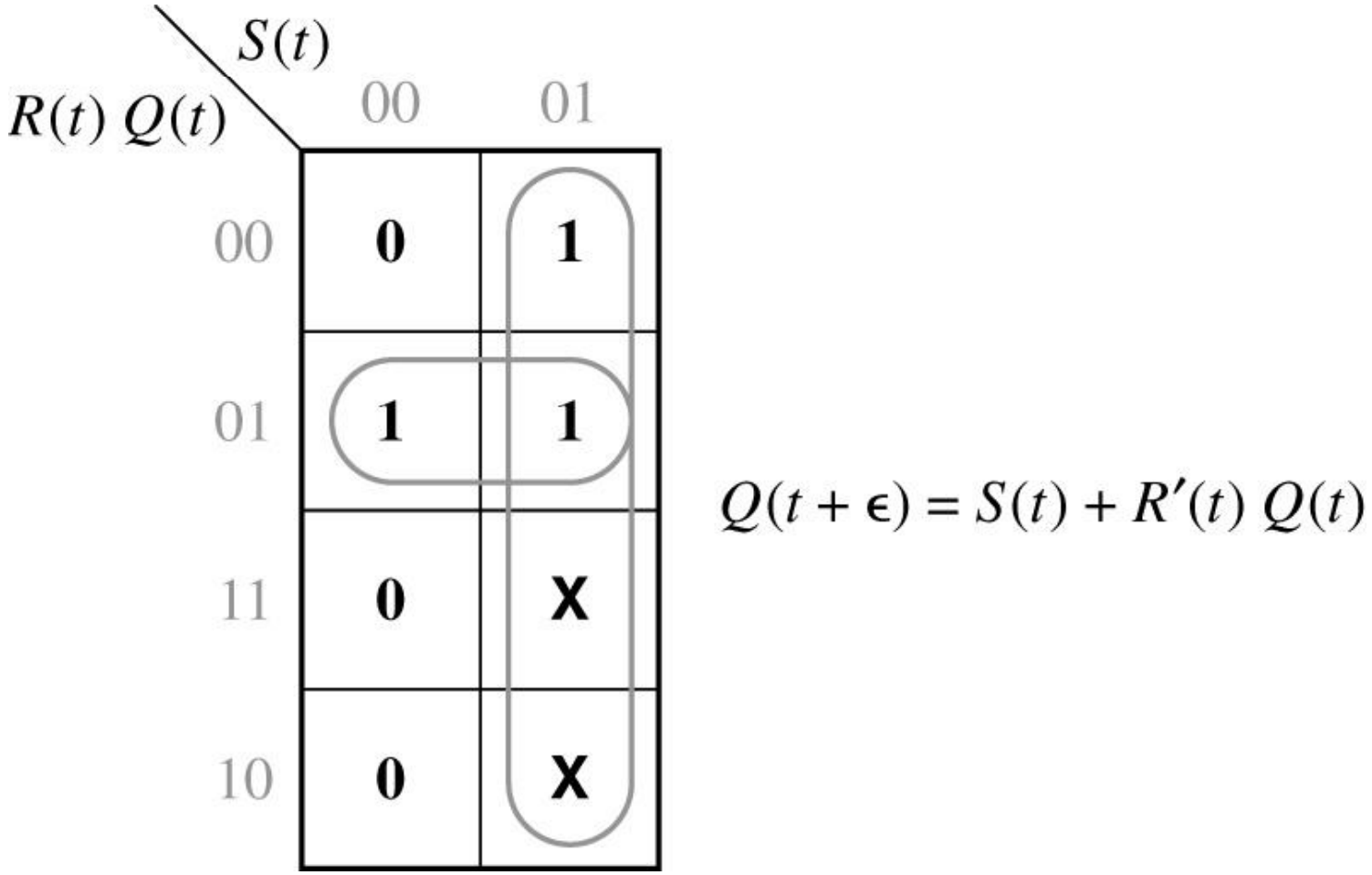


Figure 11-8: **Map for Q(*t* + E)**

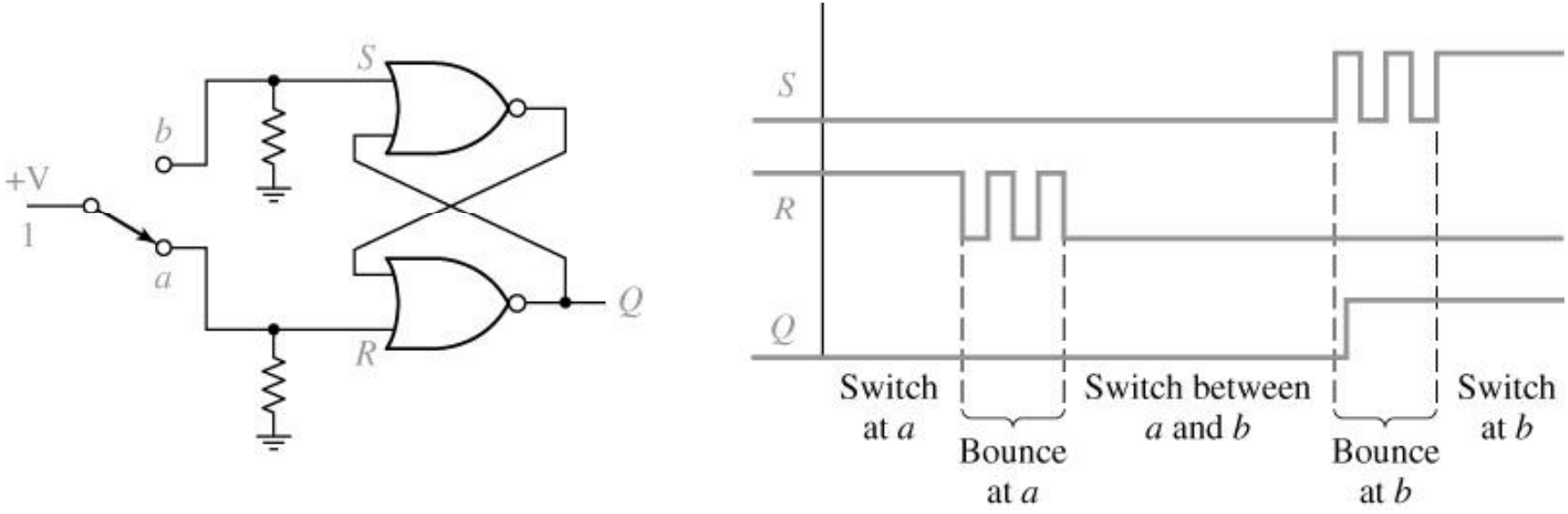


Figure 11-9: **Switch Debouncing with an S-R Latch**

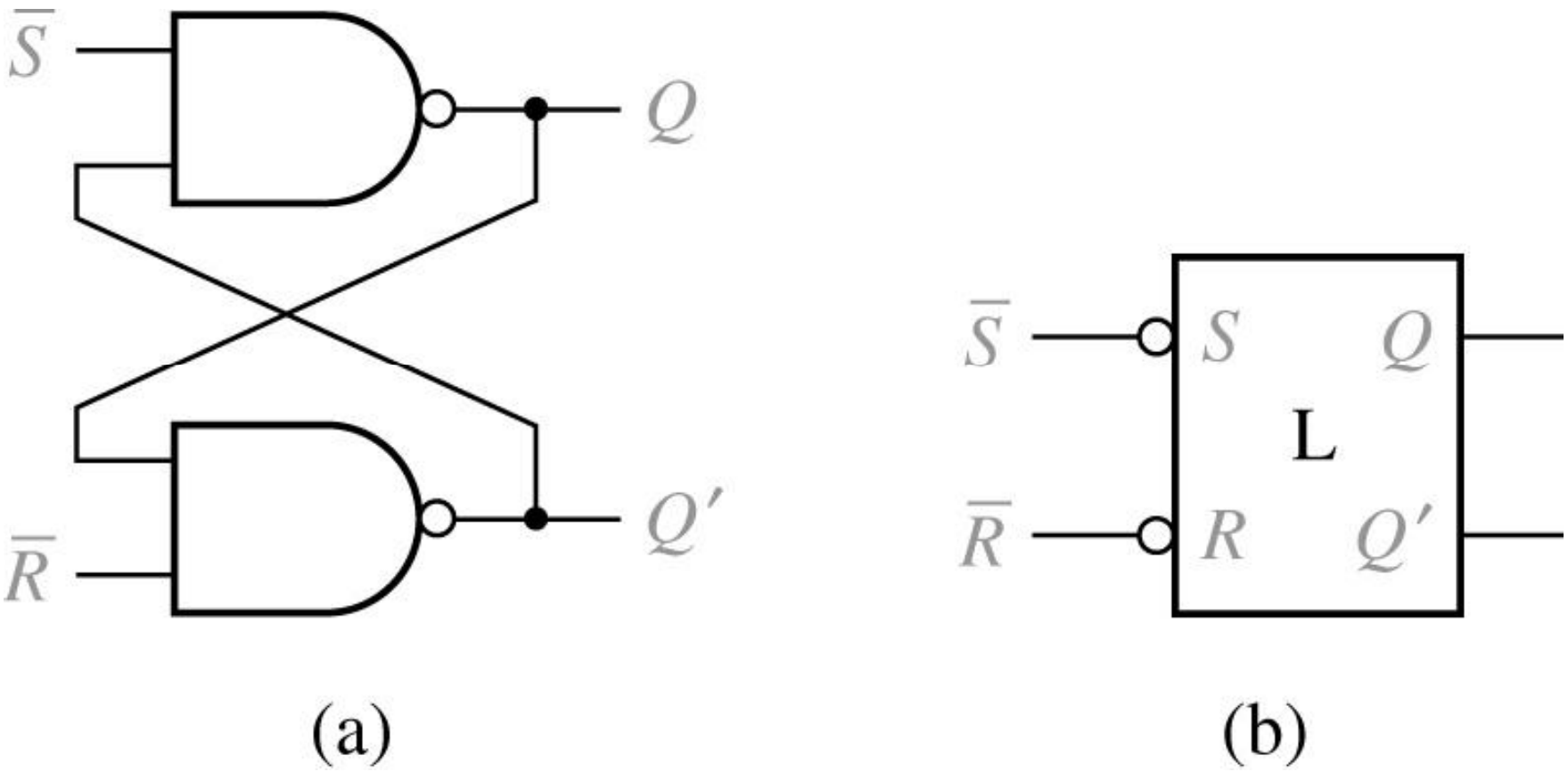


Figure 11-10: **$\overline{S}$-$\overline{R}$ Latch**

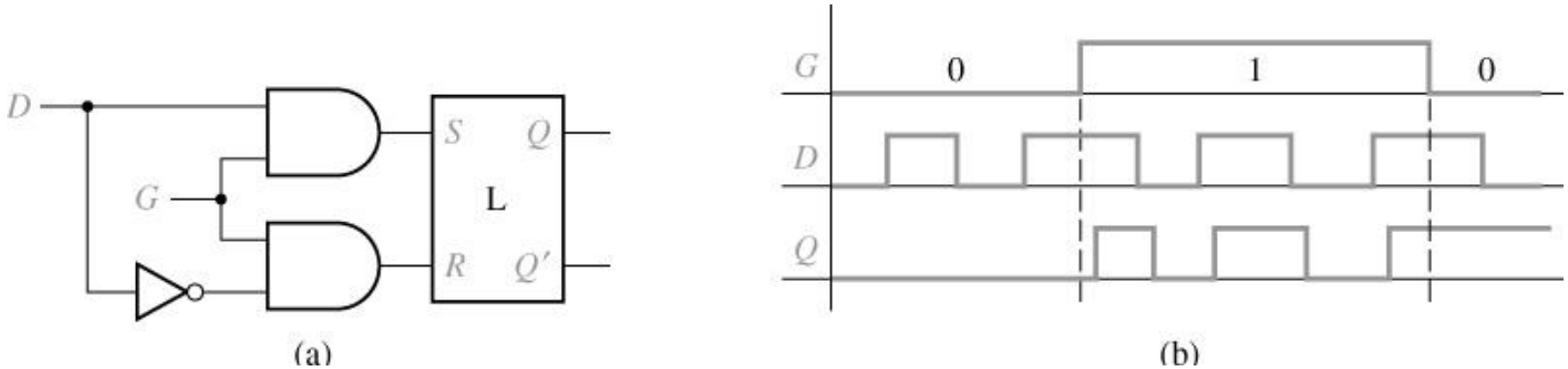


Figure 11-11: **Gated D Latch**

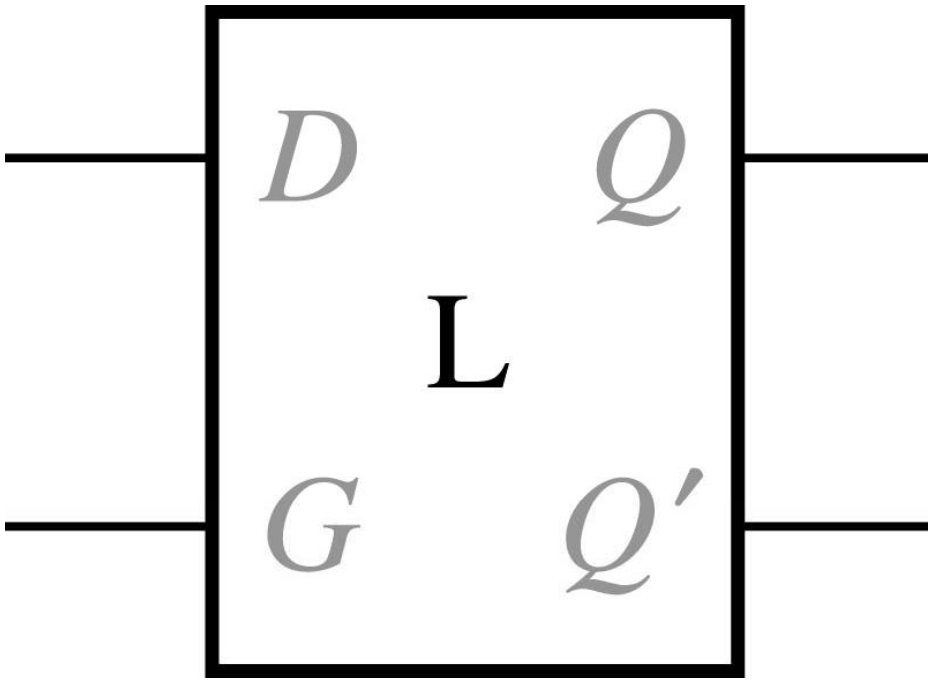


Figure 11-12 (left): **Symbol and Truth Table for Gated Latch**

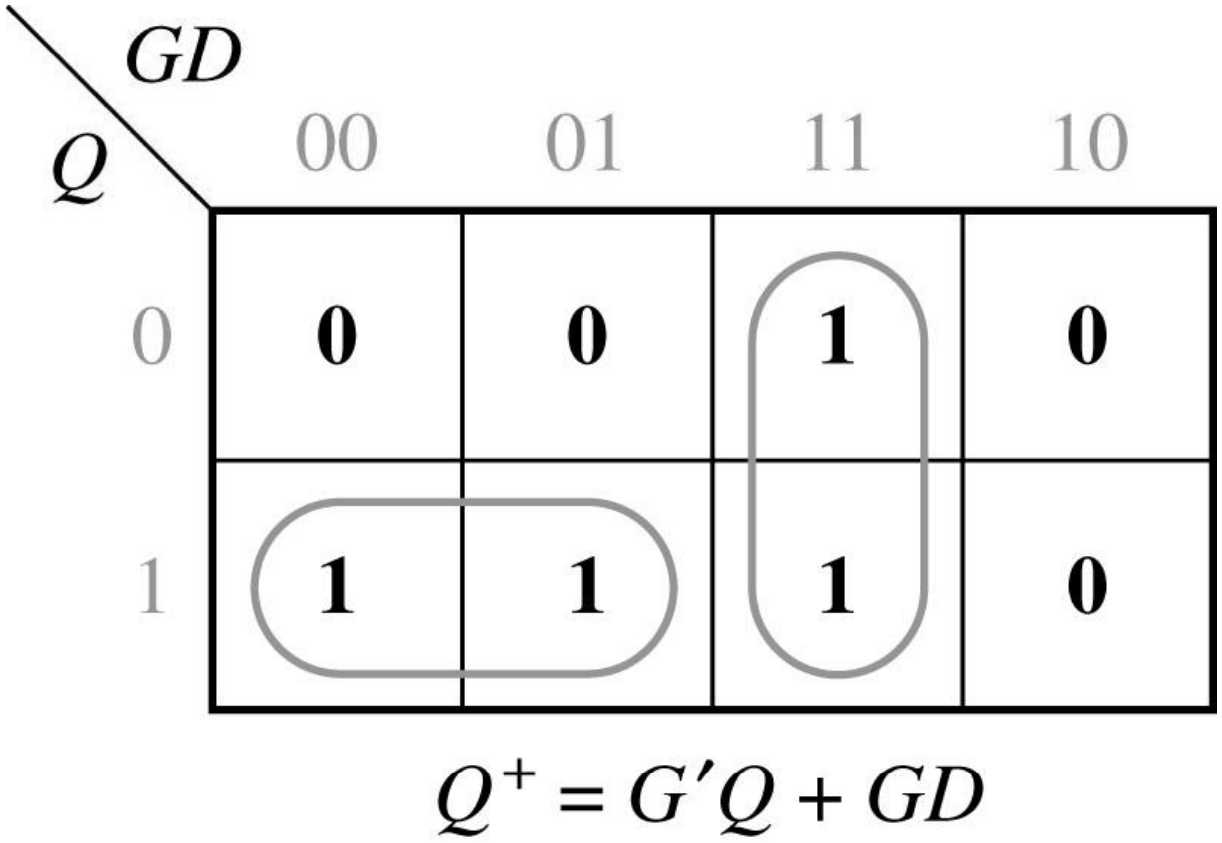
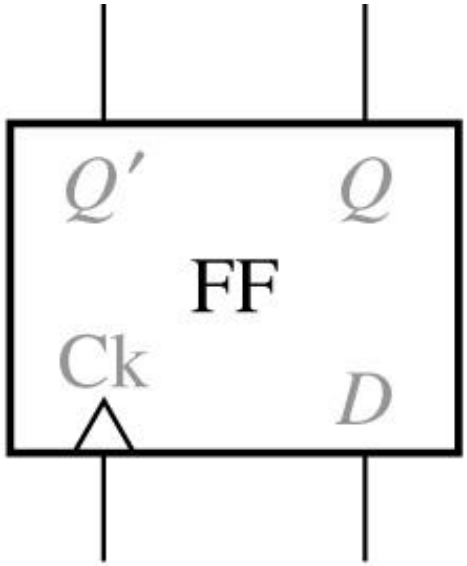
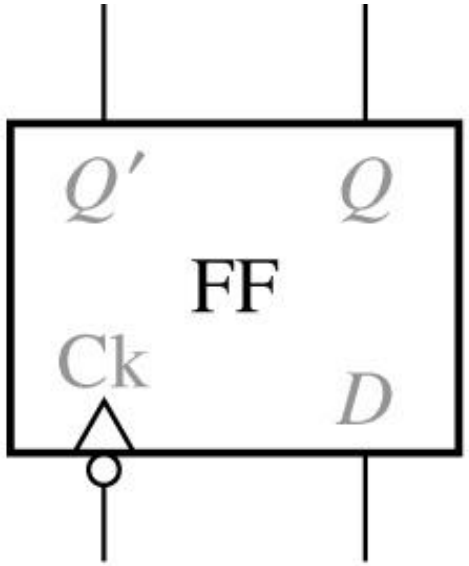


Figure 11-12 (right): **Symbol and Truth Table for Gated Latch**



(a) Rising-edge trigger



(b) Falling-edge trigger

Figure 11-13a and b: **D Flip-Flops**

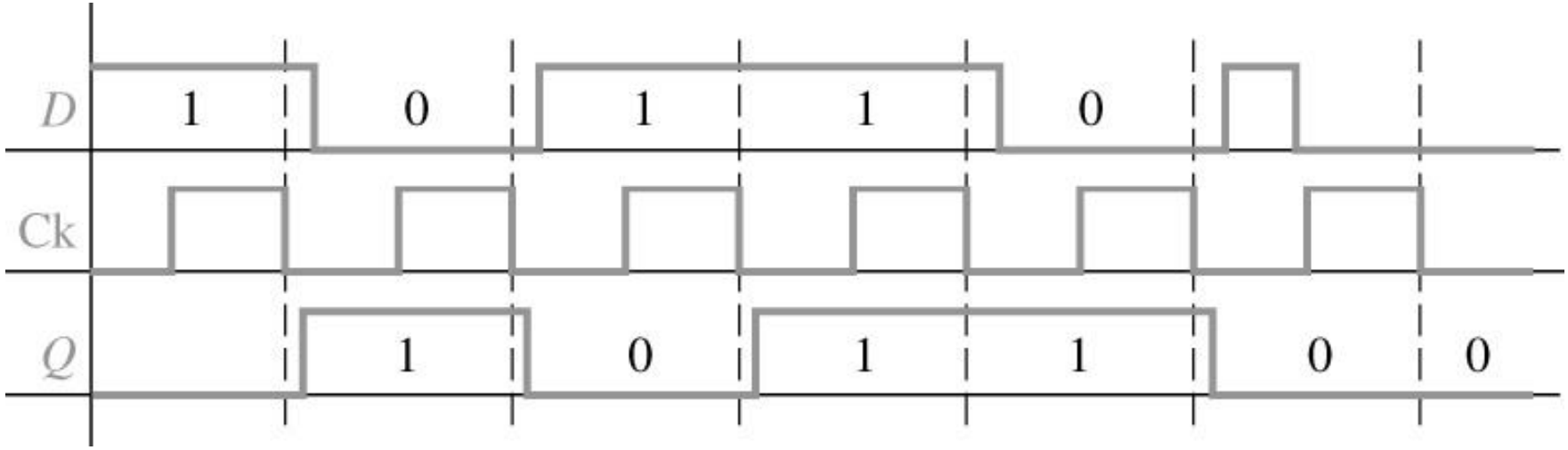
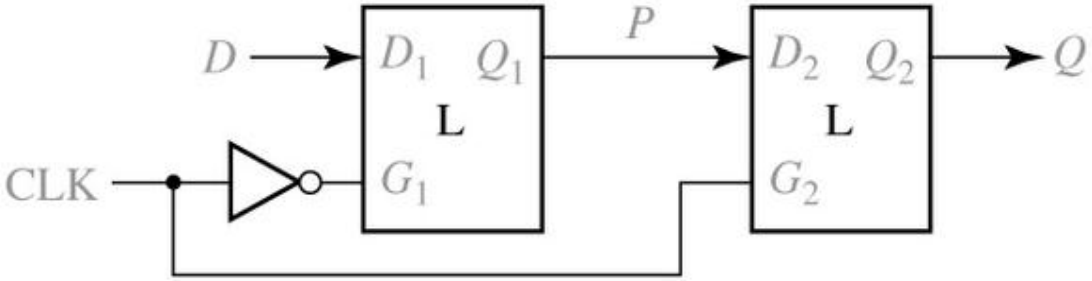
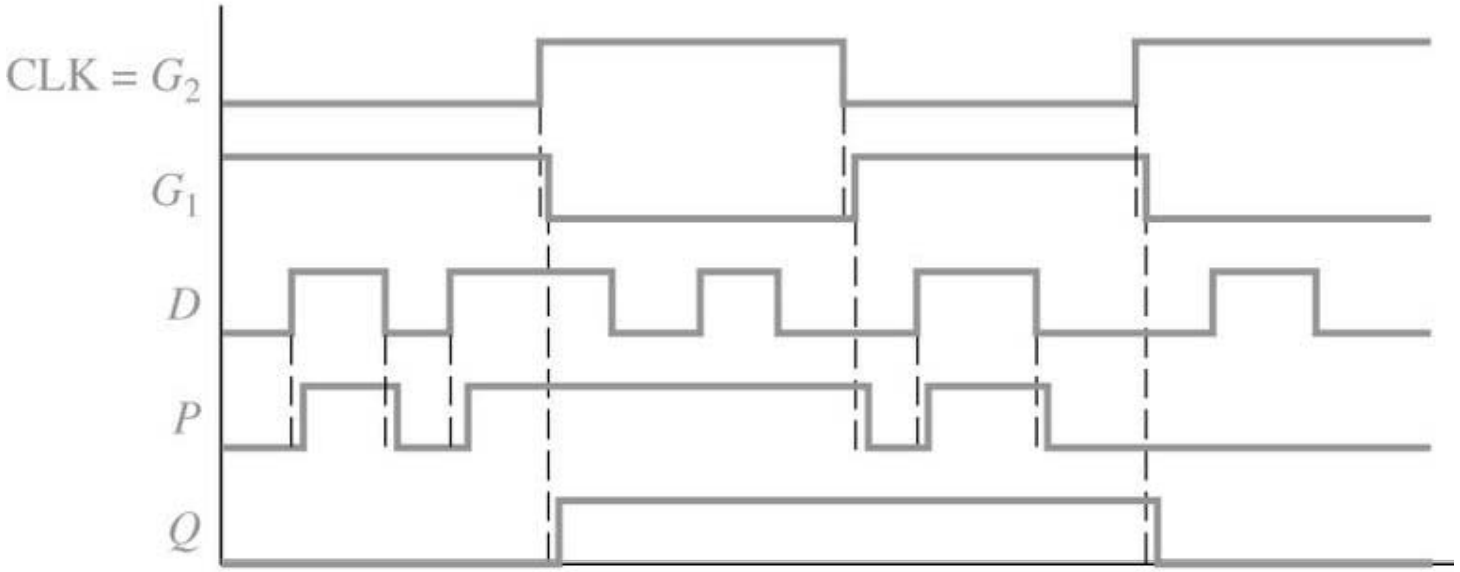


Figure 11-14: **Timing for D Flip-Flop (Falling Edge Trigger)**



(a) Construction from two gated D latches



(b) Time analysis

Figure 11-15: **D Flip-Flop (Rising Edge Trigger)**

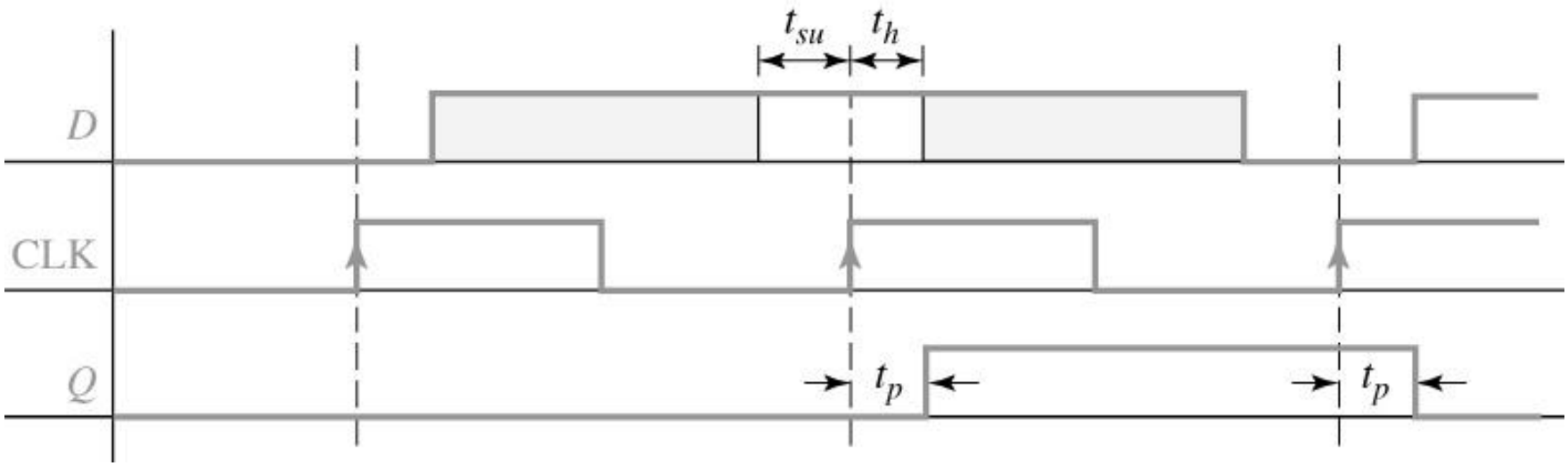


Figure 11-16: **Setup and Hold Times for an Edge-Triggered D Flip-Flop**

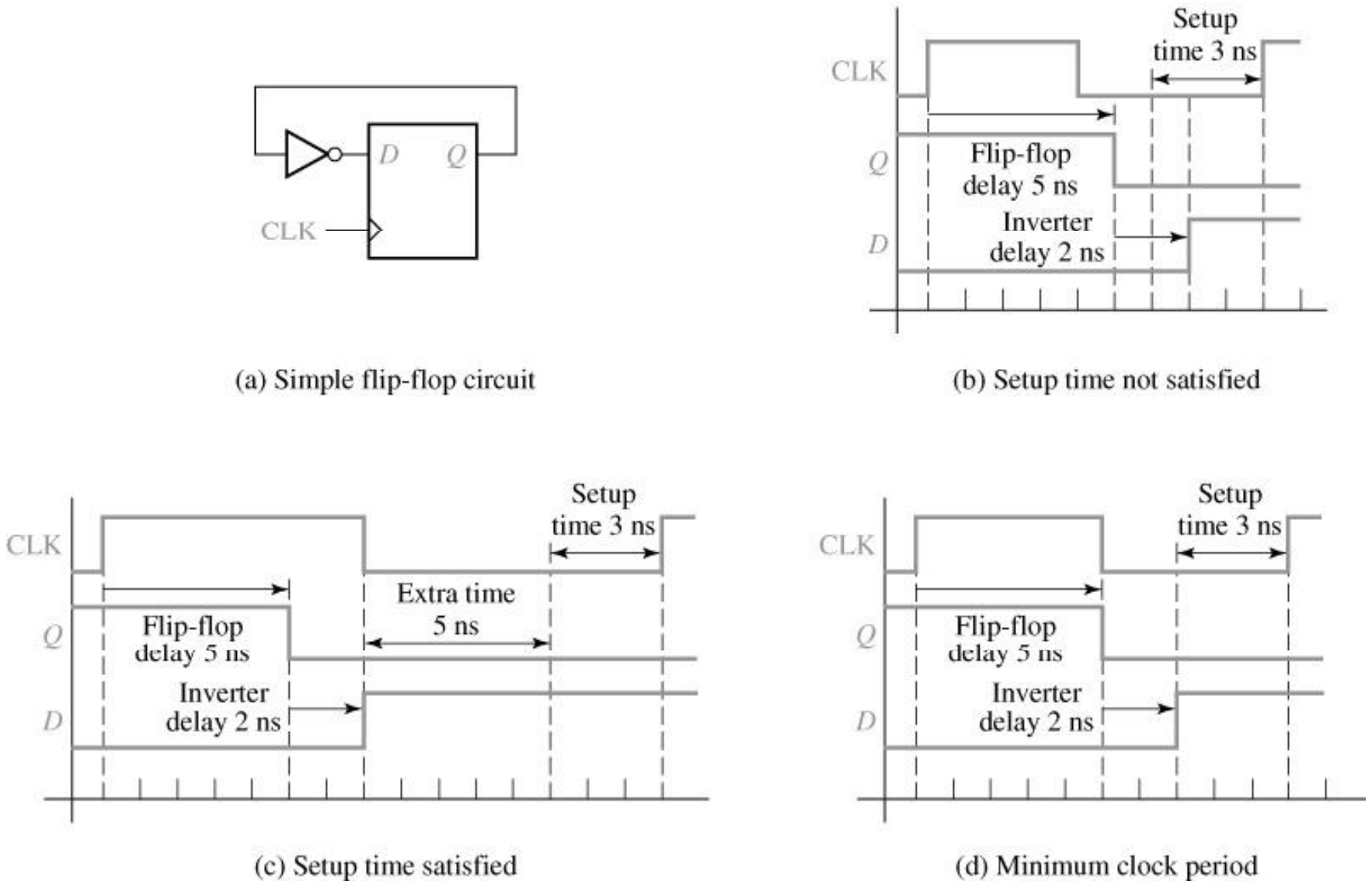


Figure 11-17: **Determination of Minimum Clock Period**

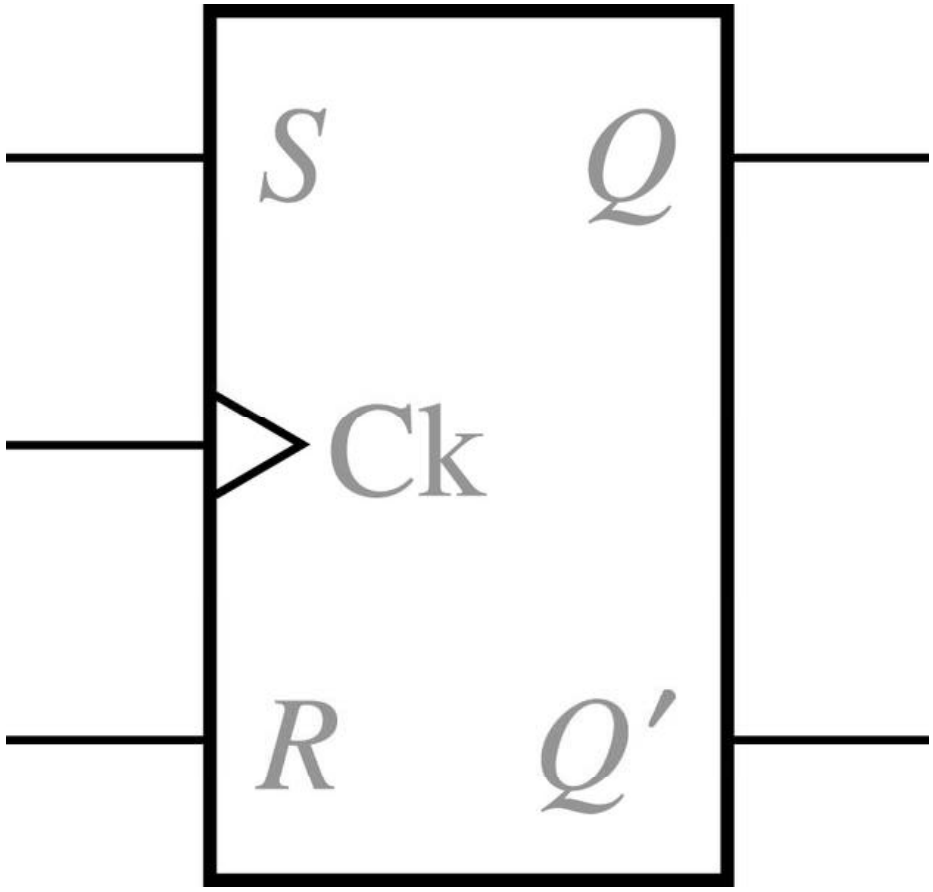
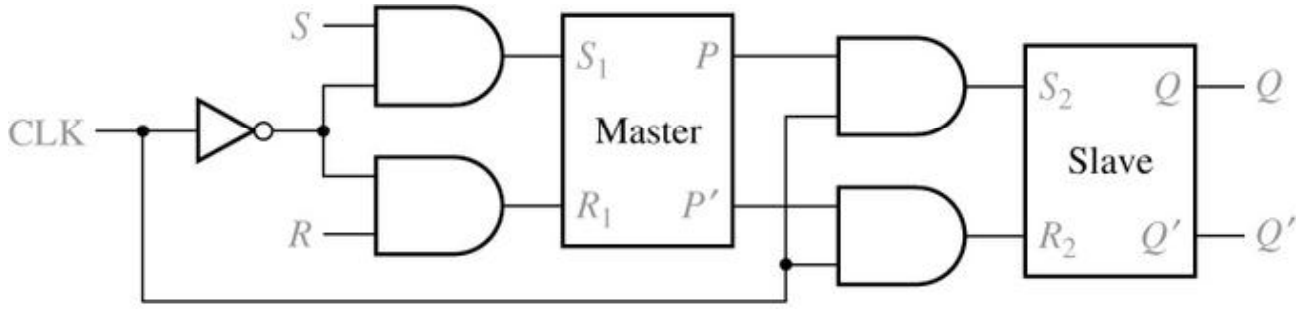
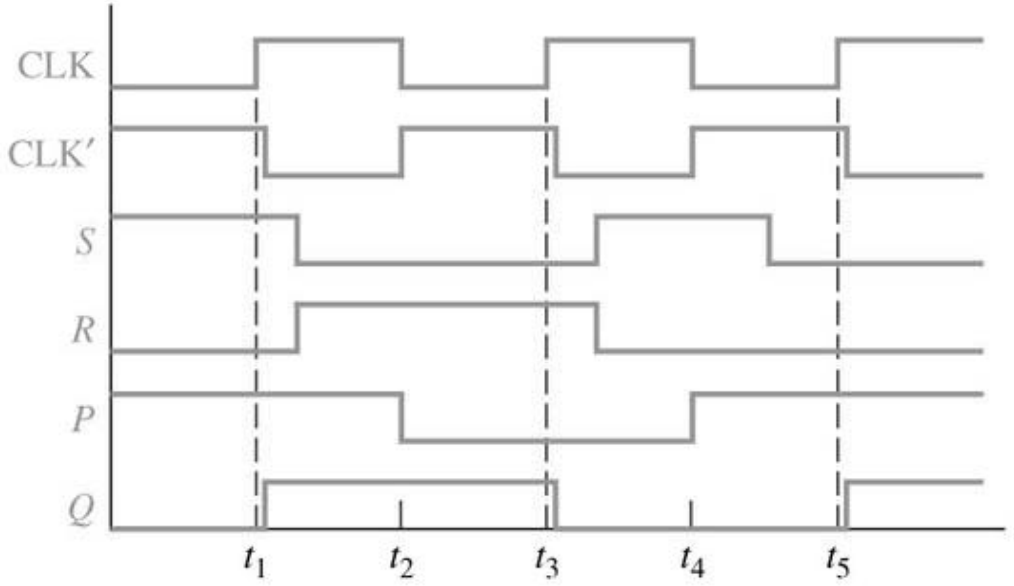


Figure 11-18: **S-R Flip-Flop**

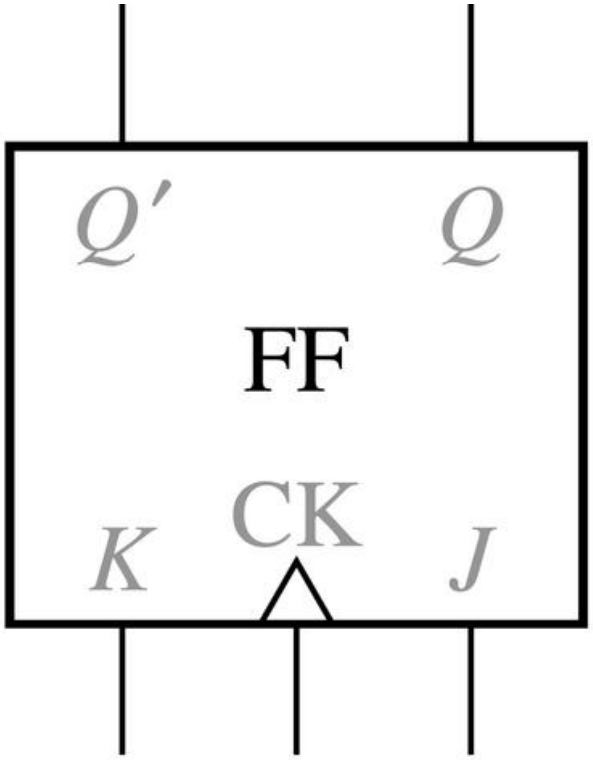


(a) Implementation with two latches



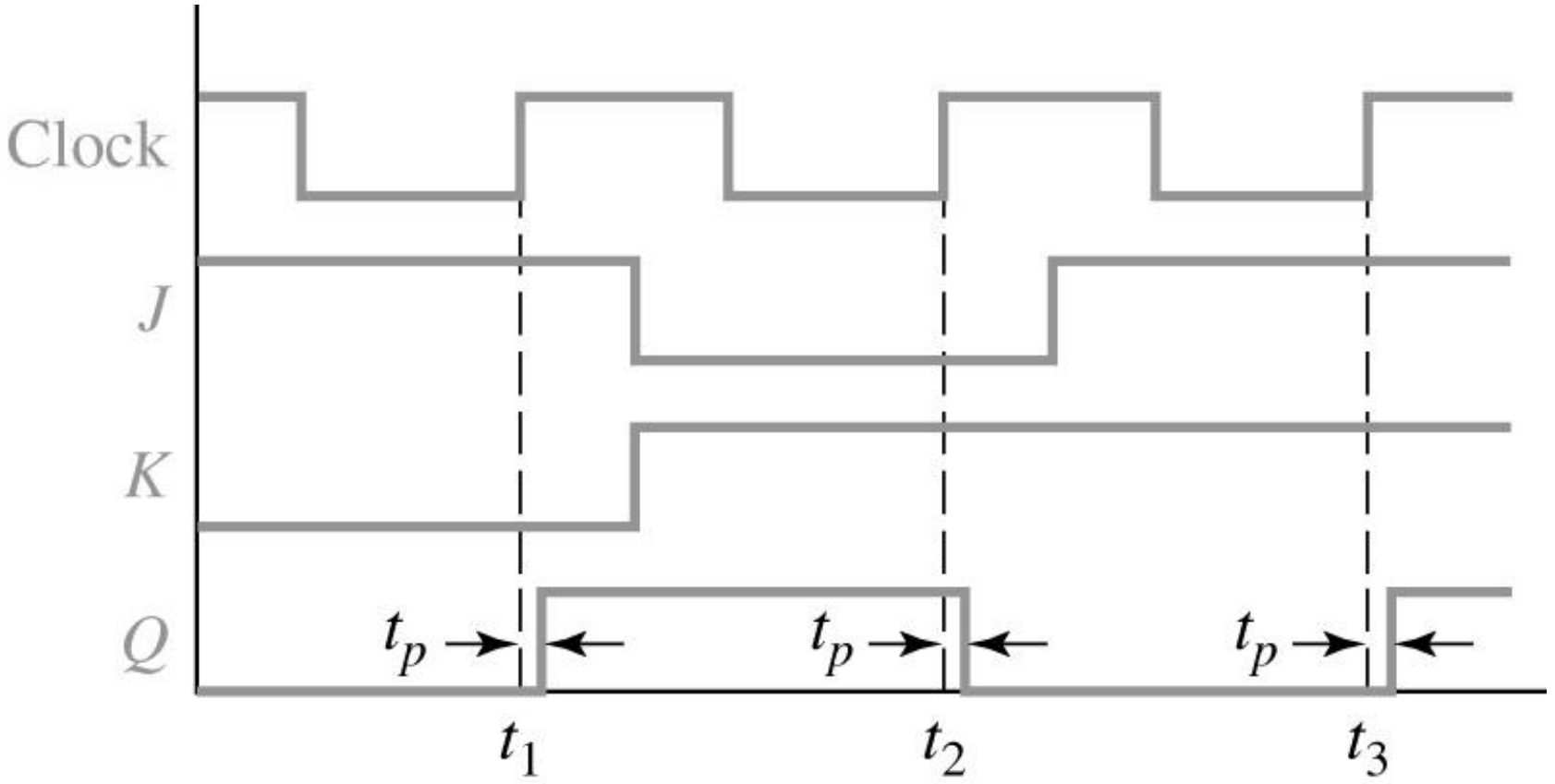
(b) Timing analysis

Figure 11-19: **S-R Flip-Flop Implementation and Timing**



(a) J-K flip-flop

Figure 11-20a: **J-K Flip-Flop (*Q* Changes on the Rising Edge)**



(c) J-K flip-flop timing

Figure 11-20c: **J-K Flip-Flop (*Q* Changes on the Rising Edge)**

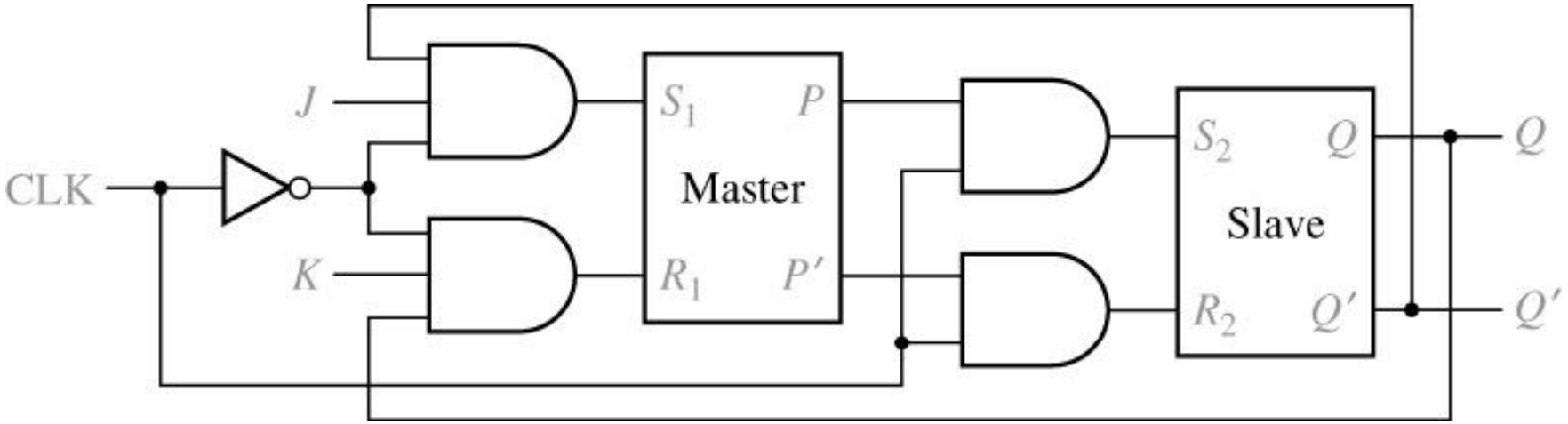
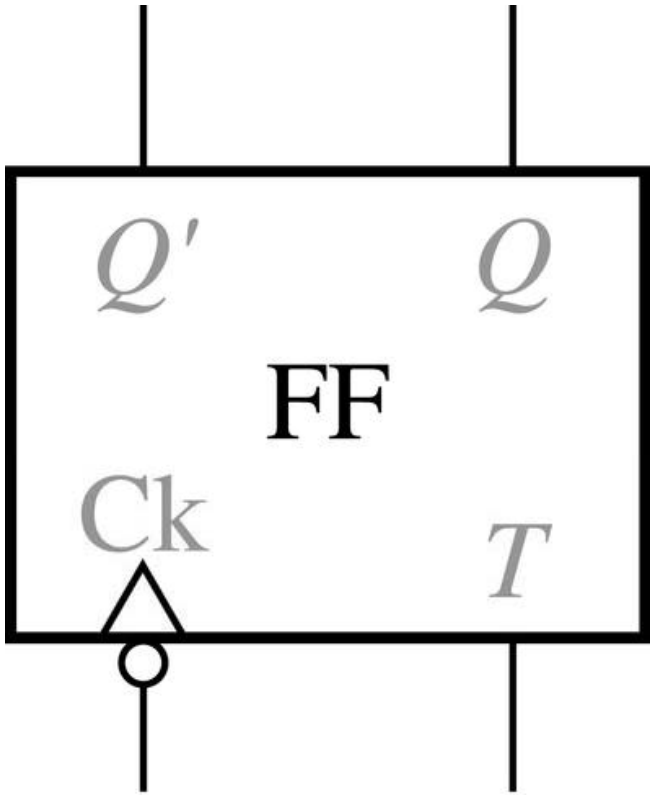


Figure 11-21: **Master-Slave J-K Flip-Flop (*Q* Changes on Rising Edge)**



(a)

Figure 11-22a: **T Flip-Flop**

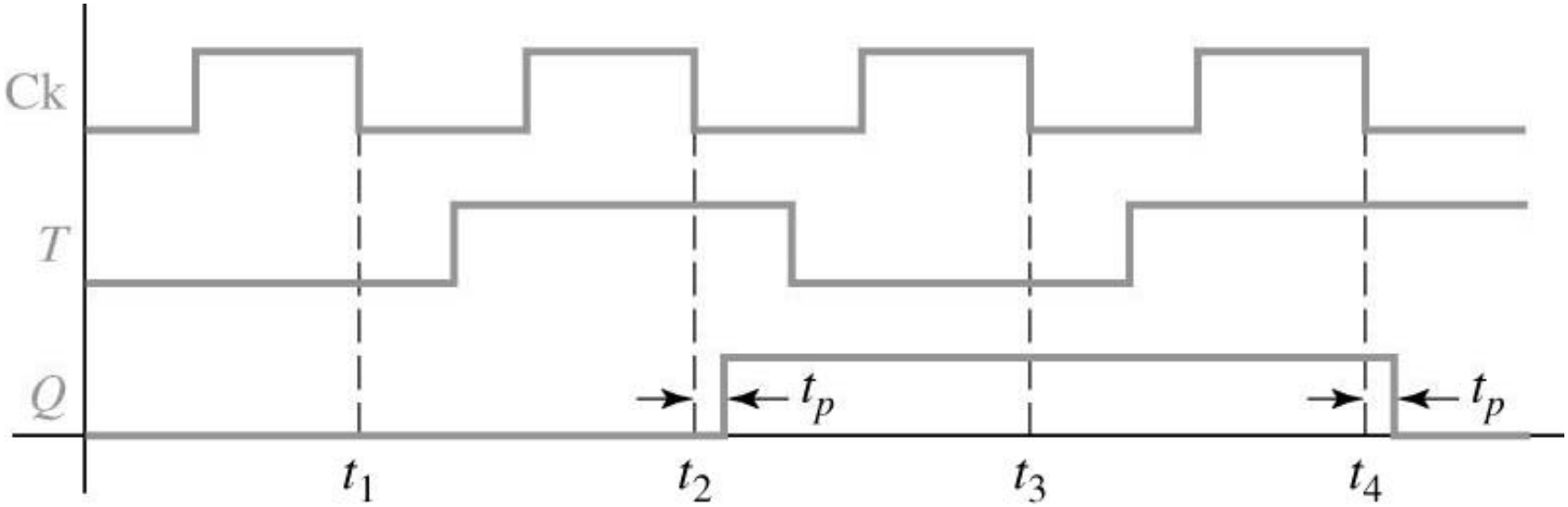
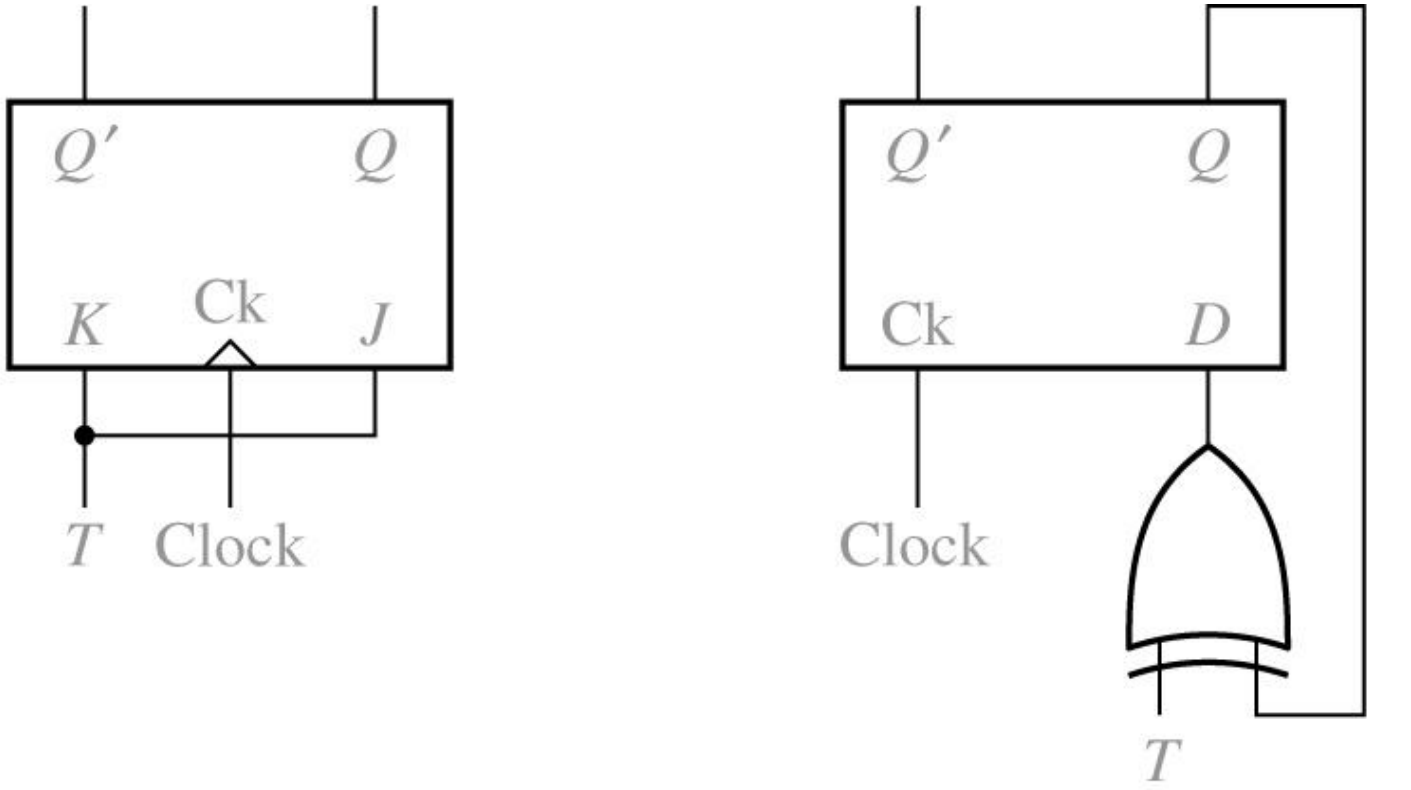


Figure 11-23: **Timing Diagram for T Flip-Flop (Falling-Edge Trigger)**



(a) Conversion of J-K to T (b) Conversion of D to T

Figure 11-24: **Implementation of T Flip-Flops**

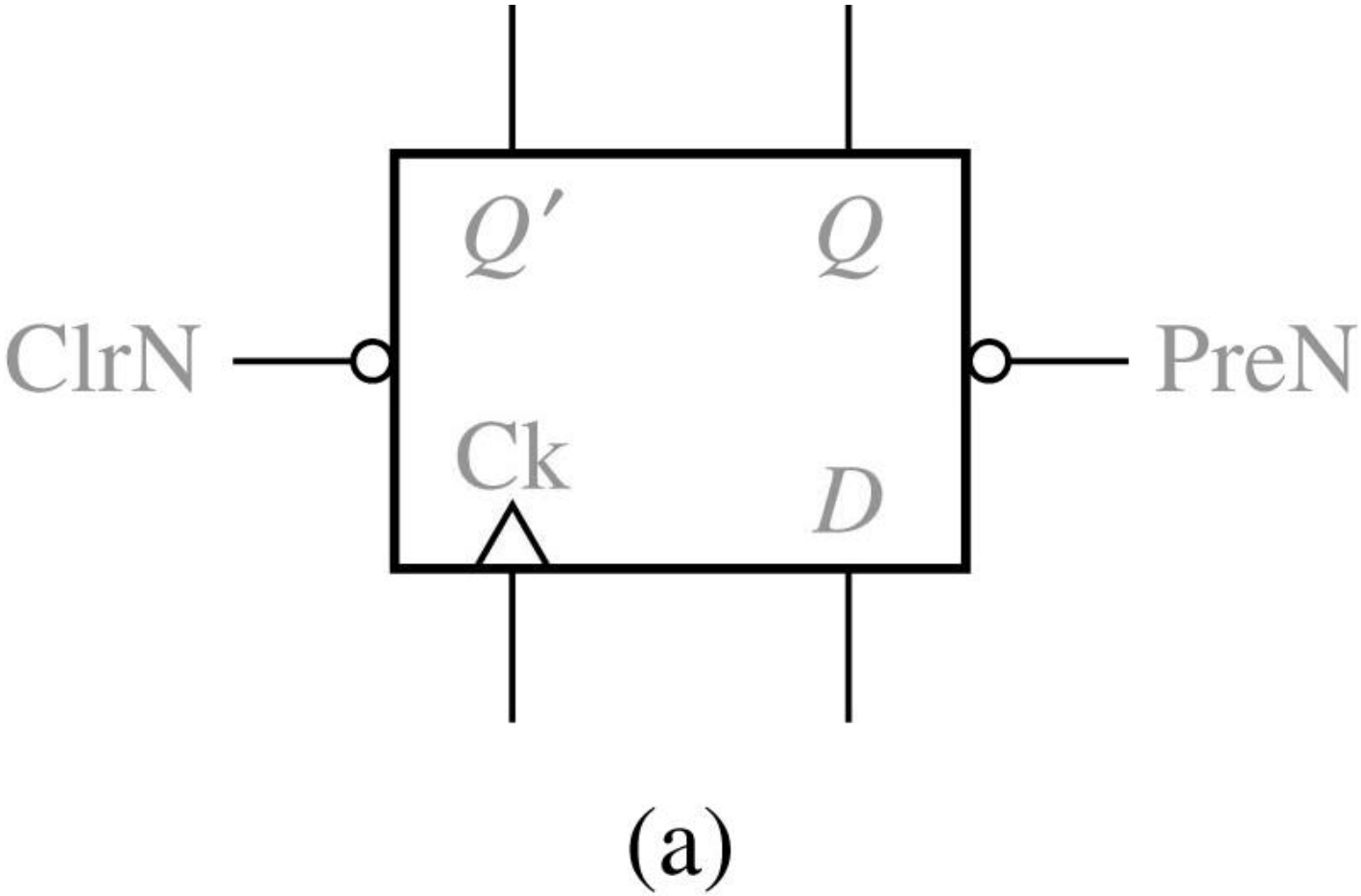


Figure 11-25: **D Flip-Flop with Clear and Preset**

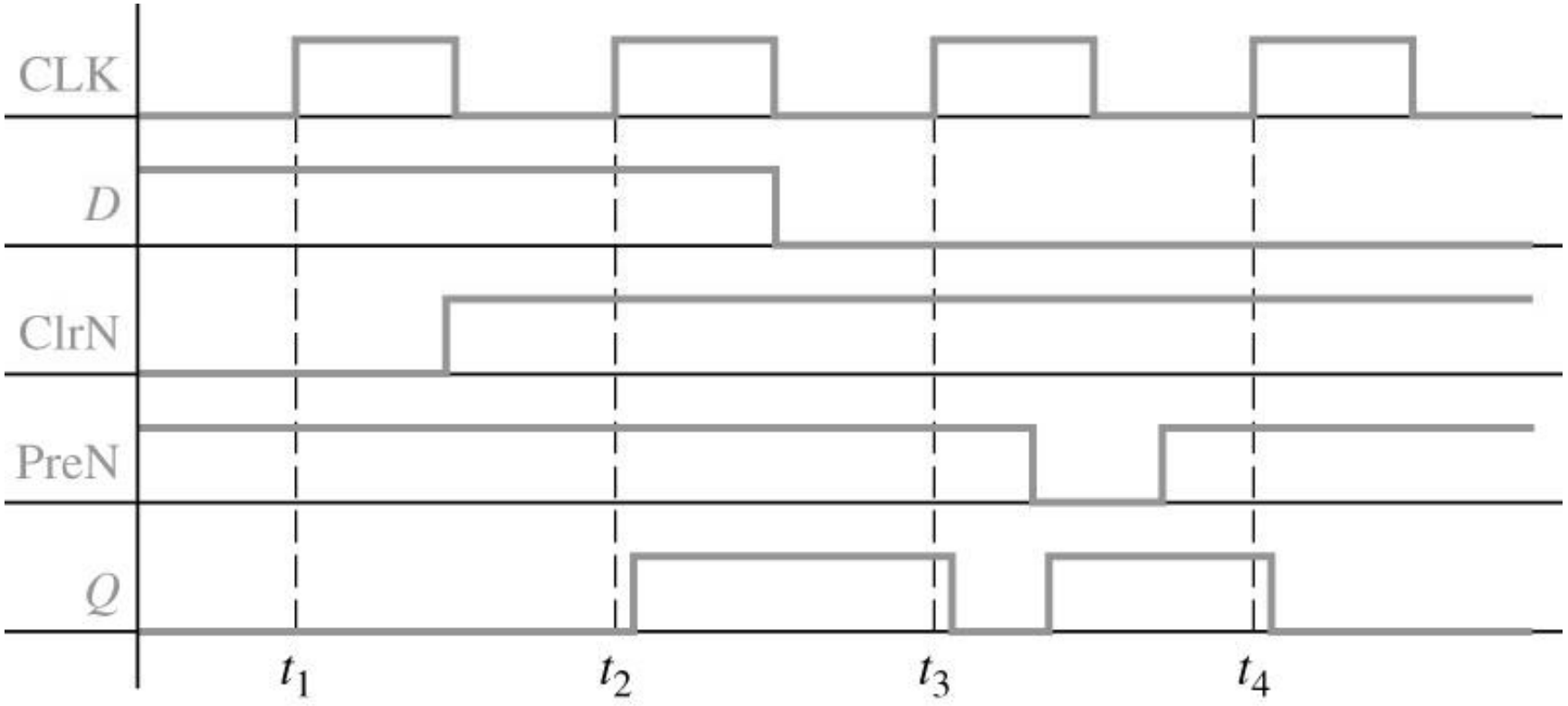


Figure 11-26: **Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset**

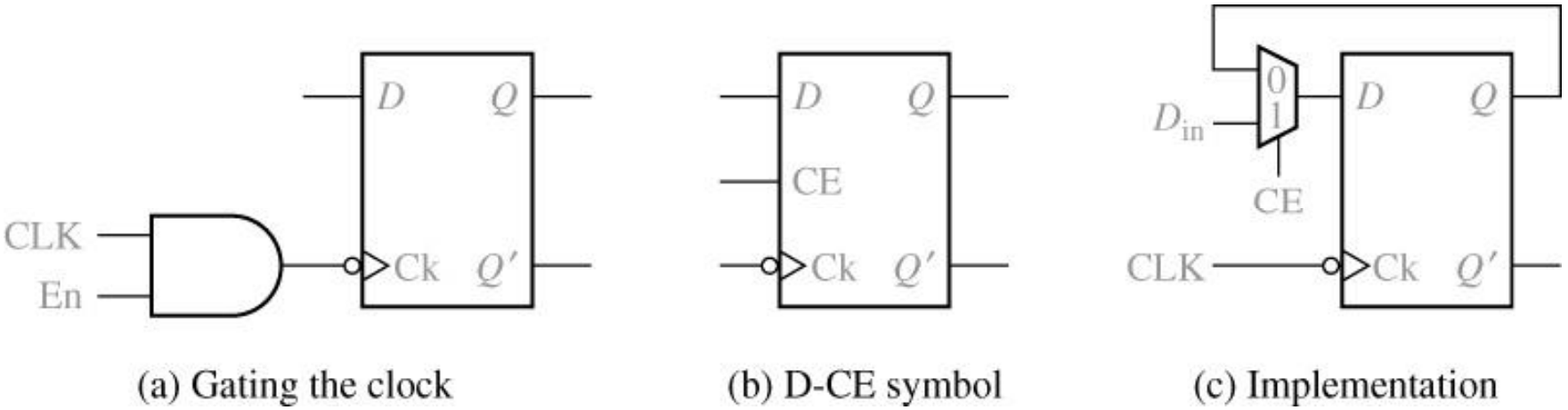
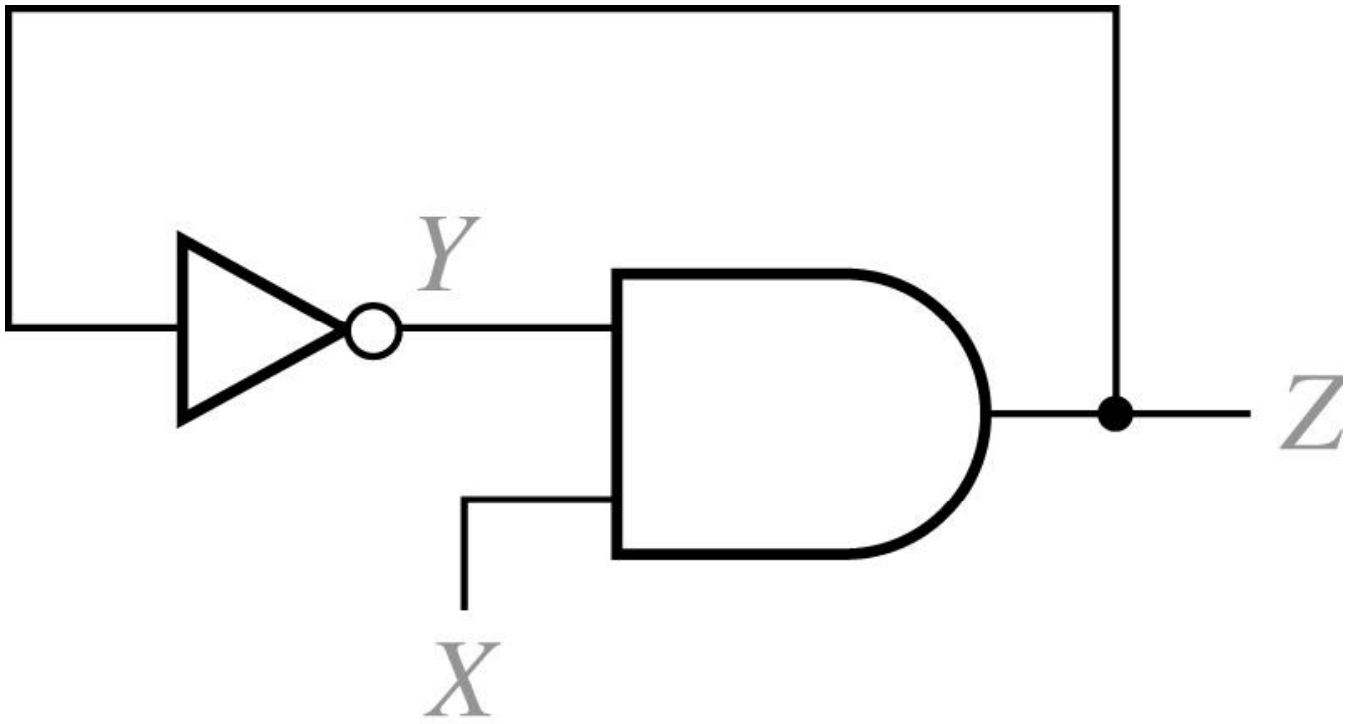
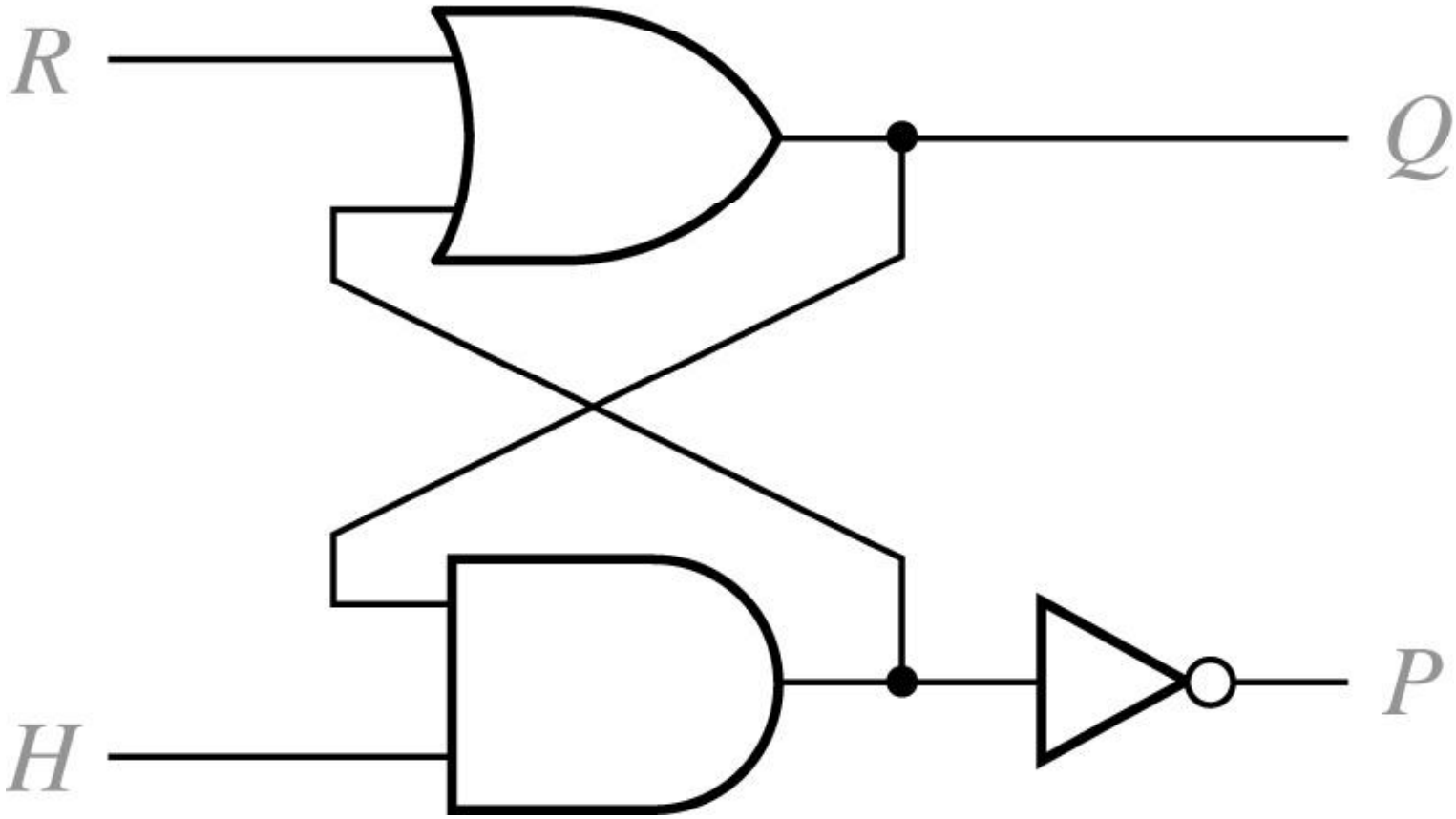


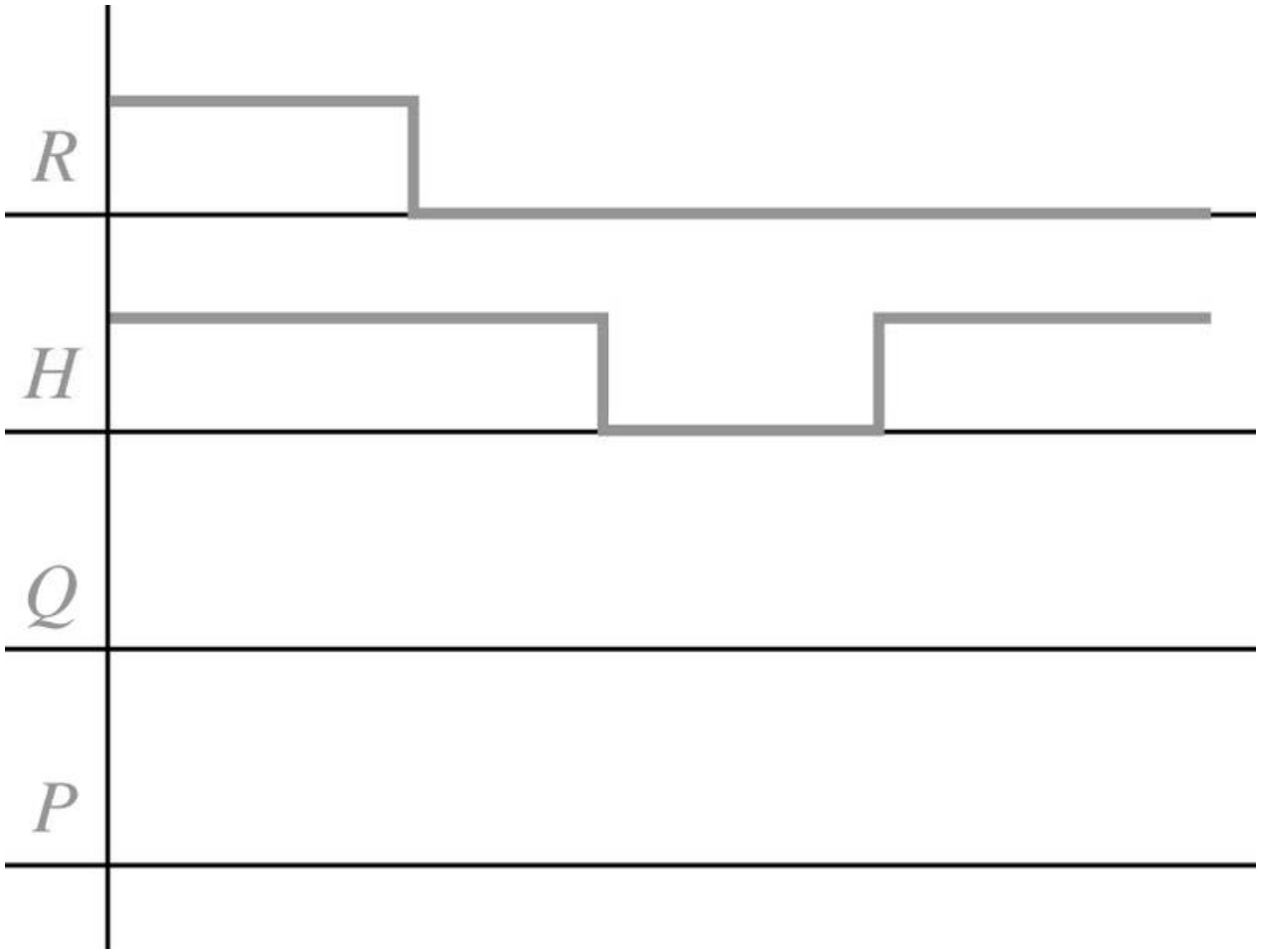
Figure 11-27: **D Flip-Flop with Clock Enable**



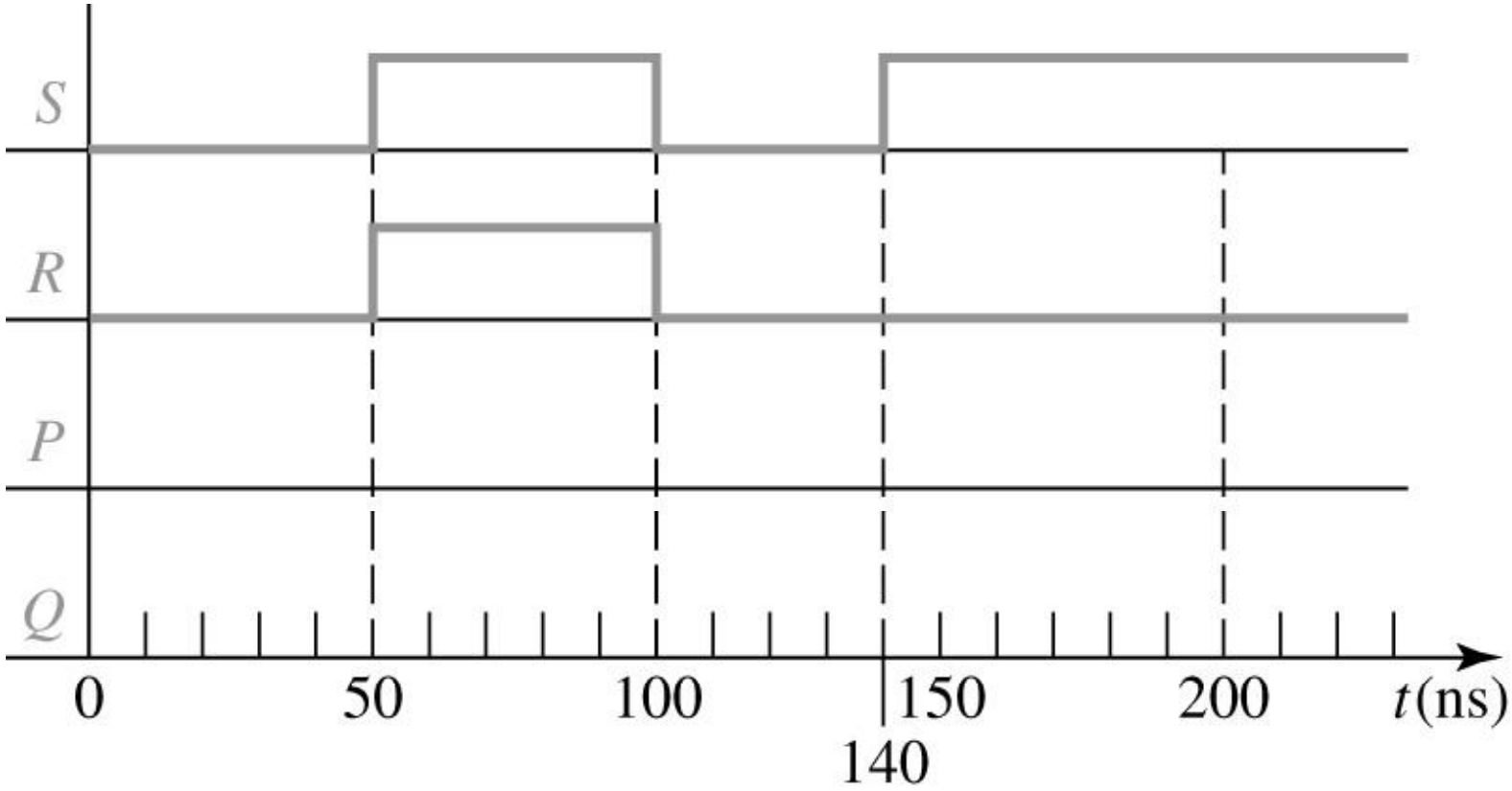
Problem 11.1



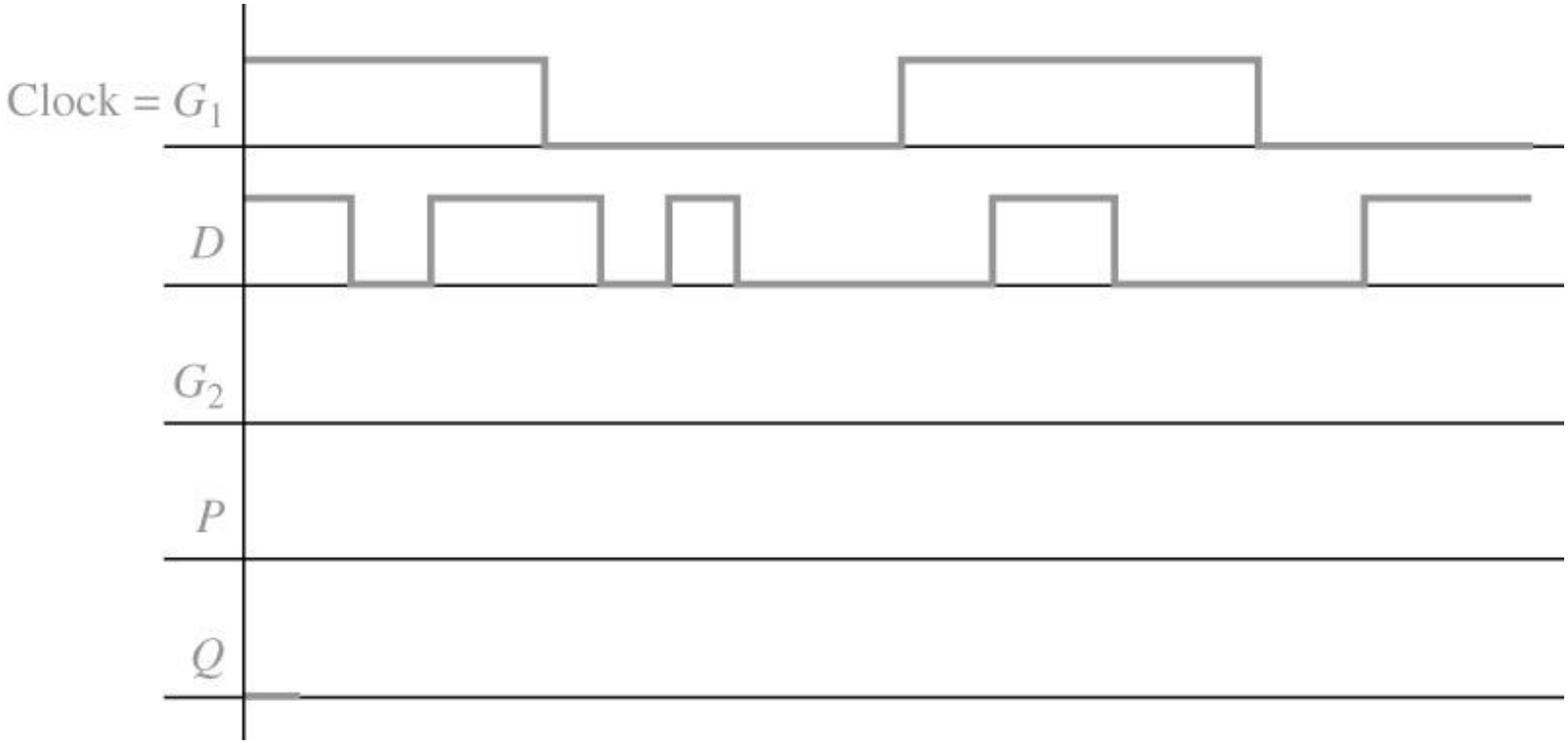
Problem 11.2b



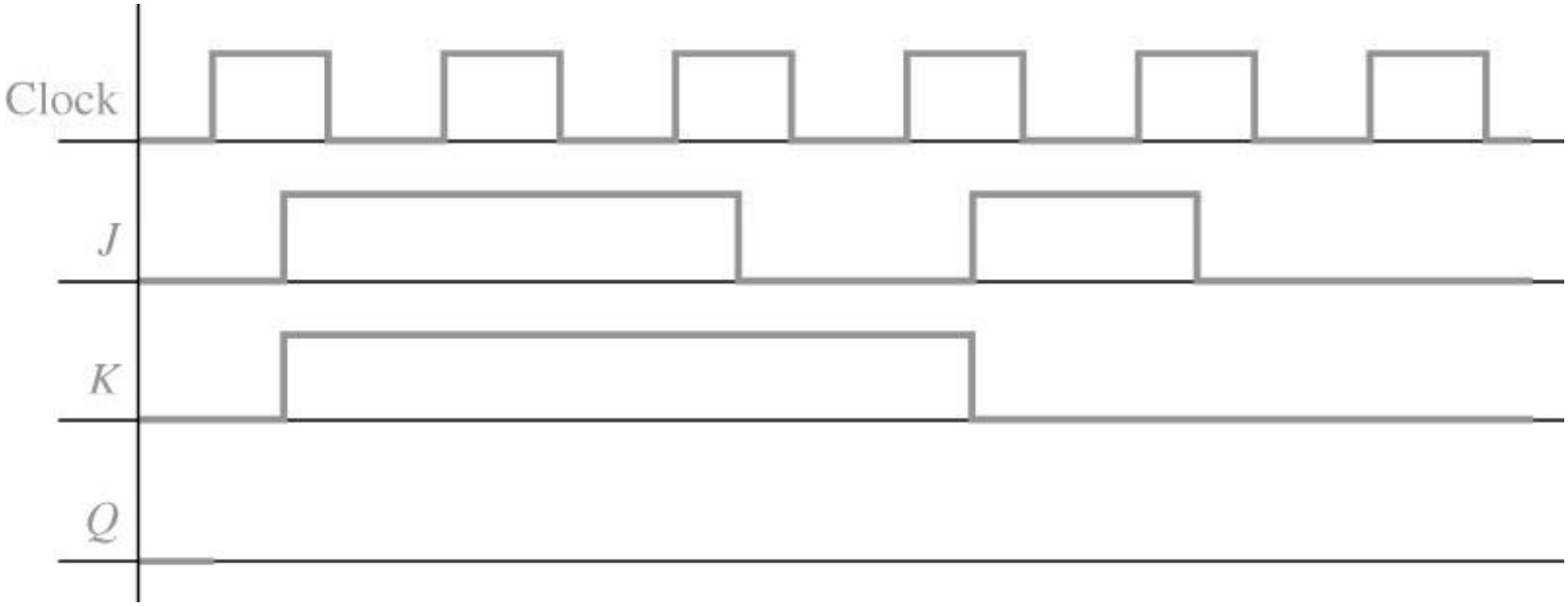
Problem 11.2c



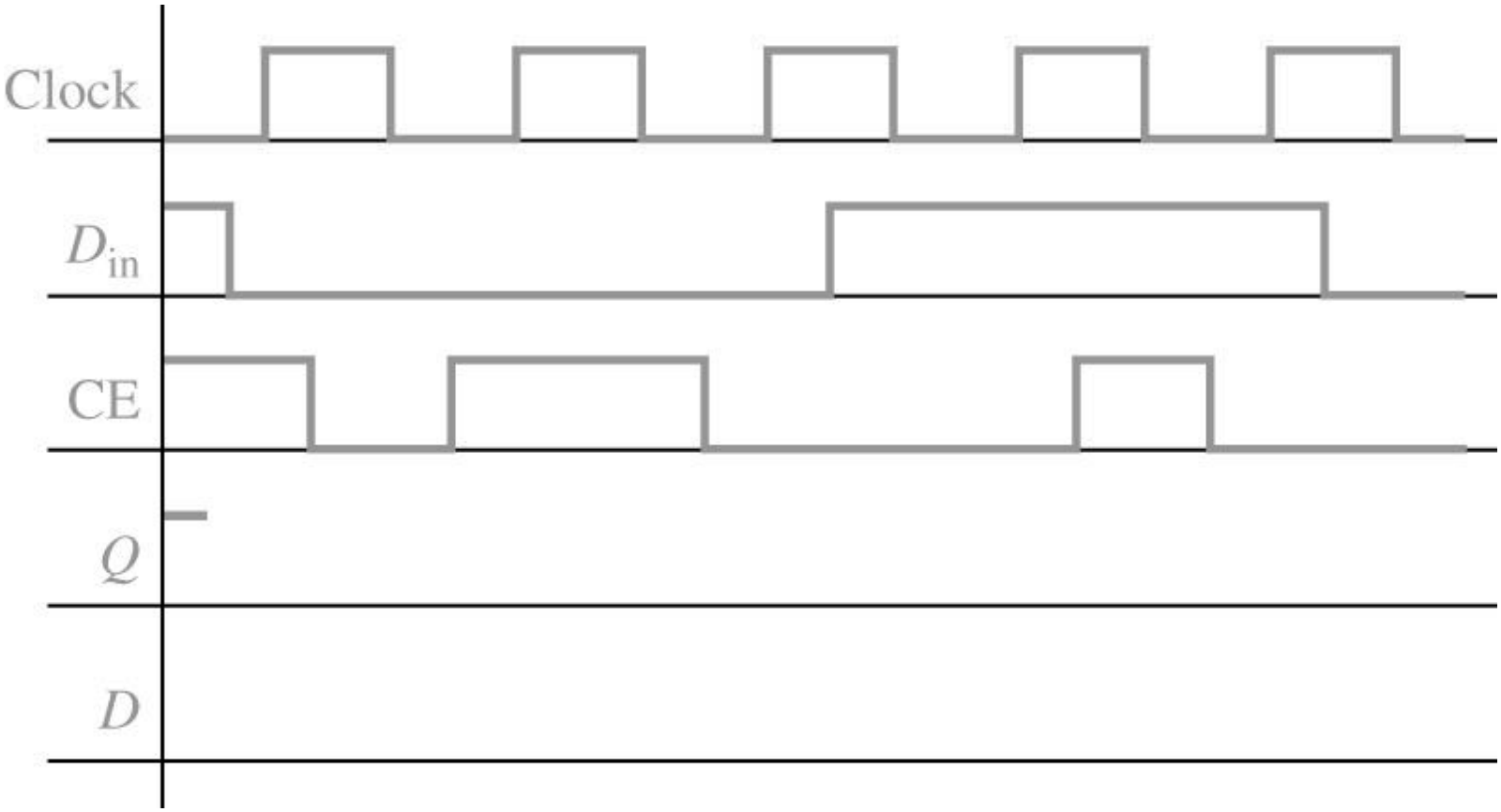
Problem 11.3



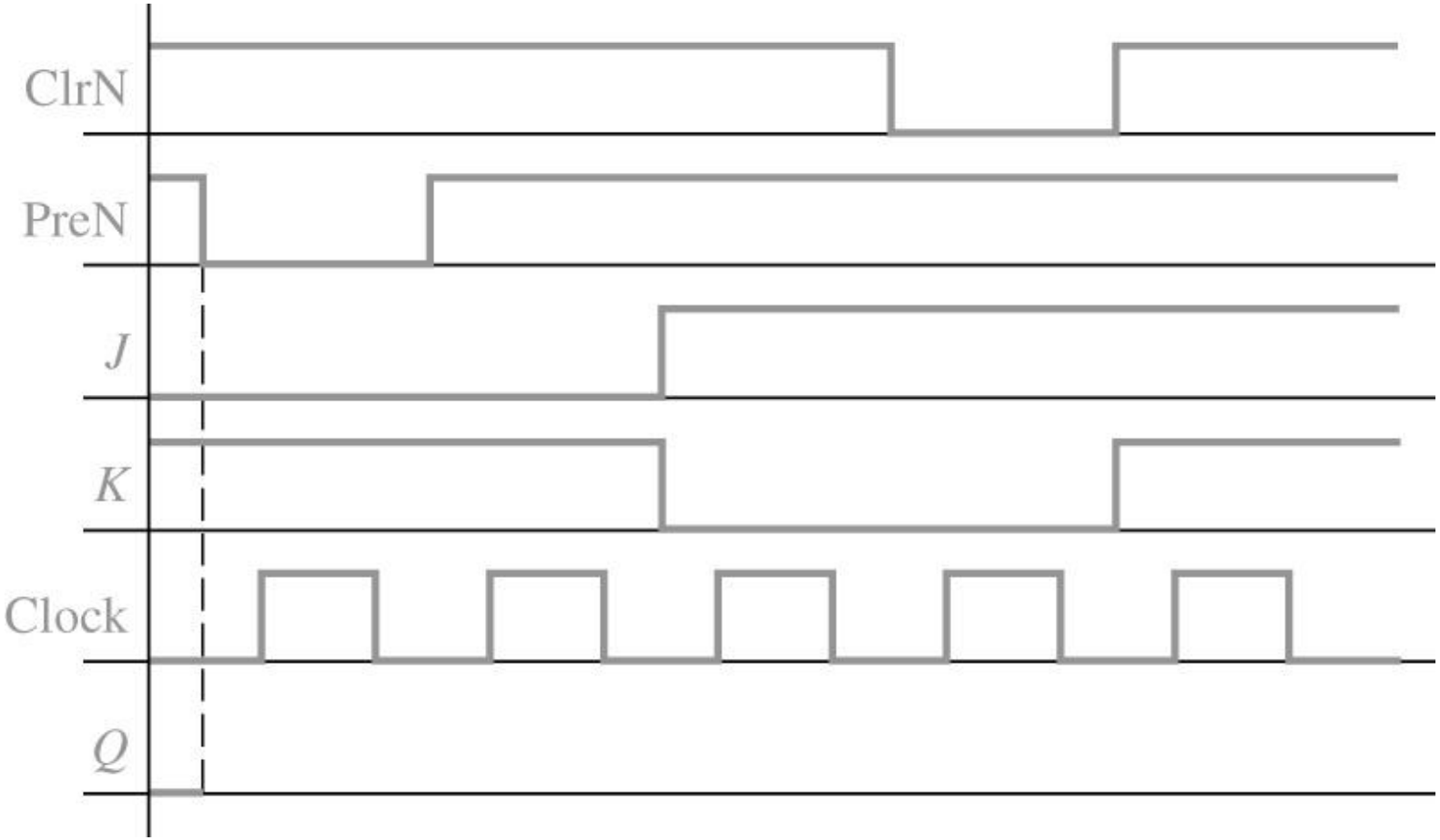
Problem 11.5



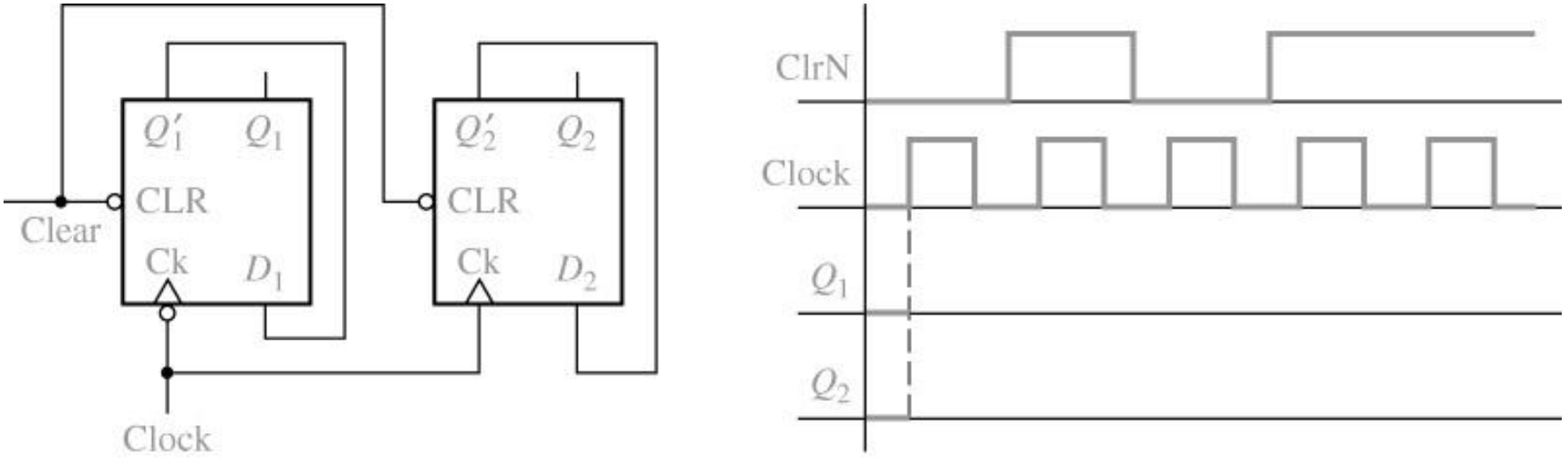
Problem 11.7



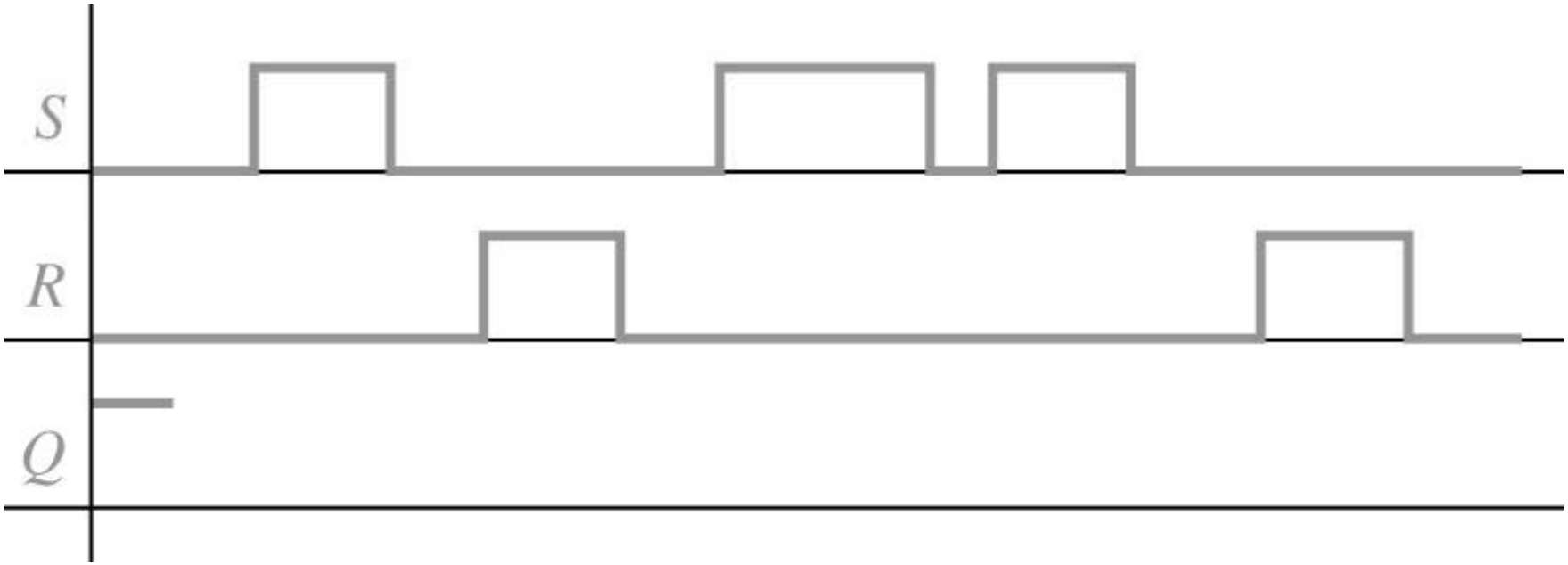
Problem 11.8



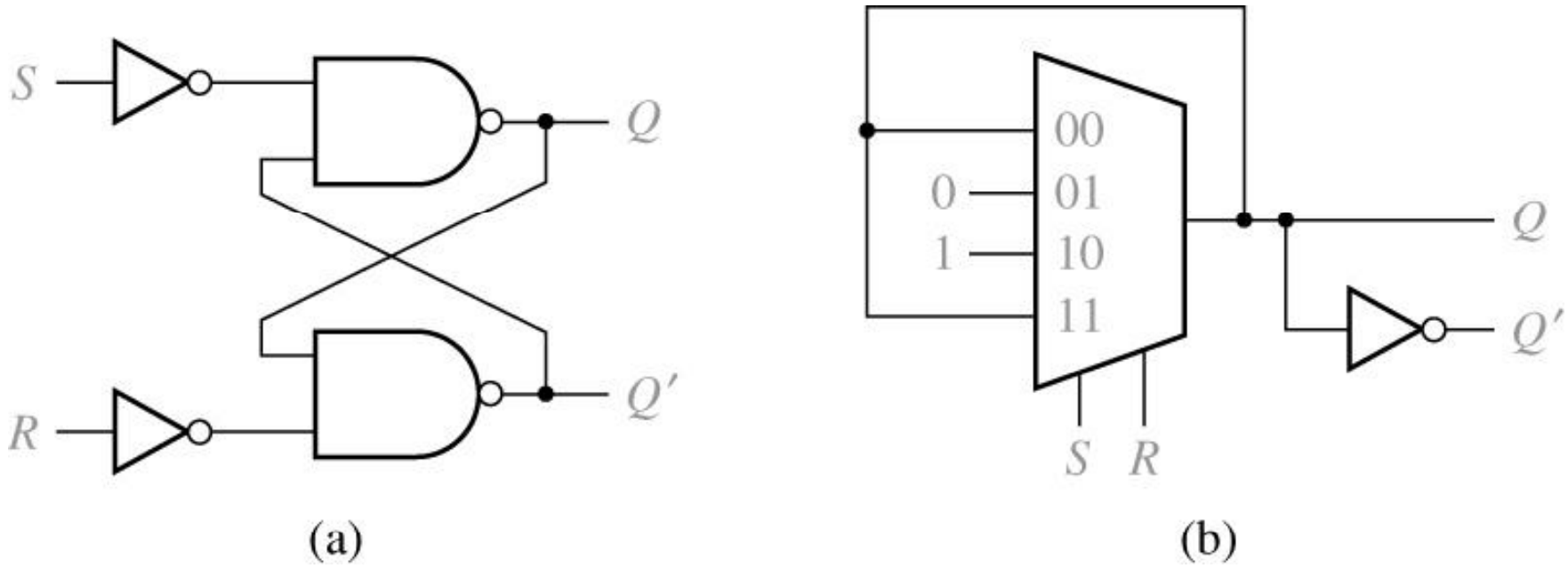
Problem 11.9a



Problem 11.9b

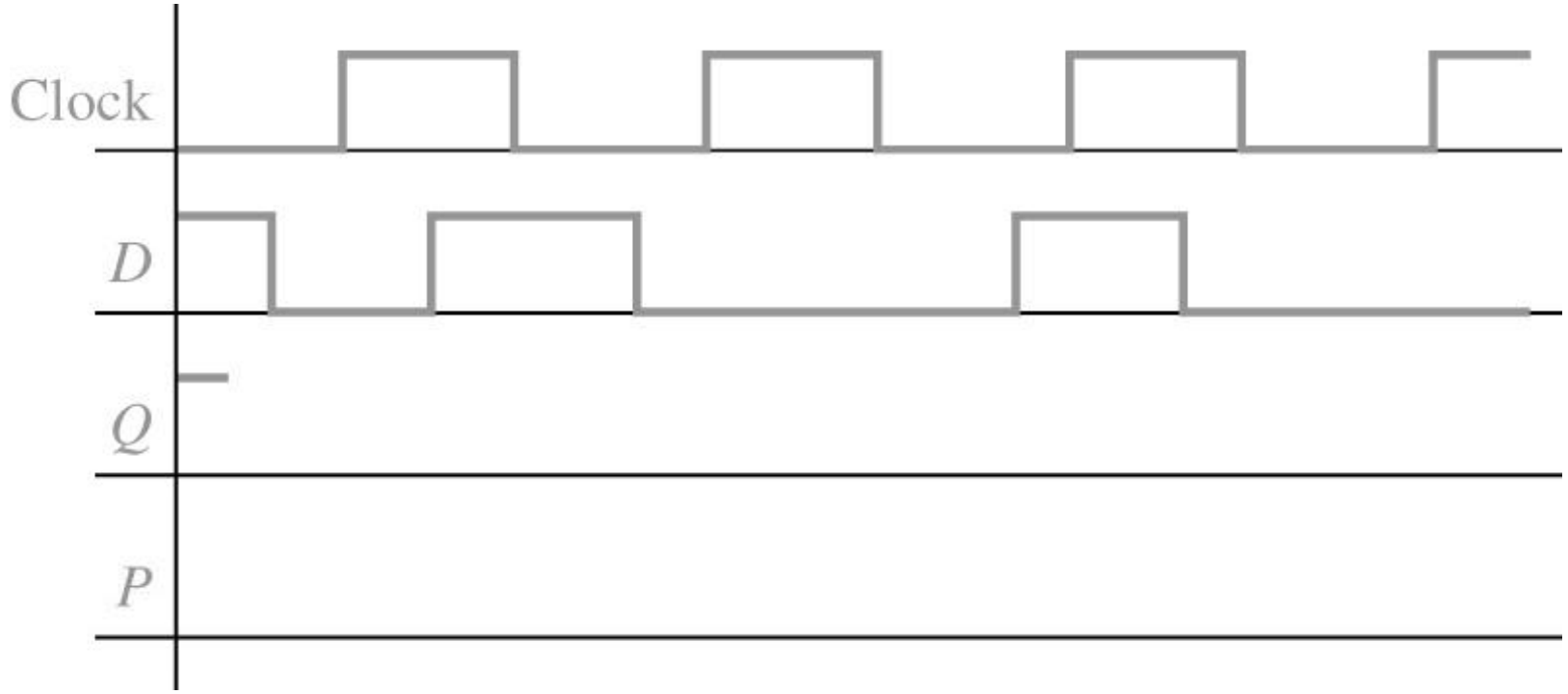


Problem 11.11

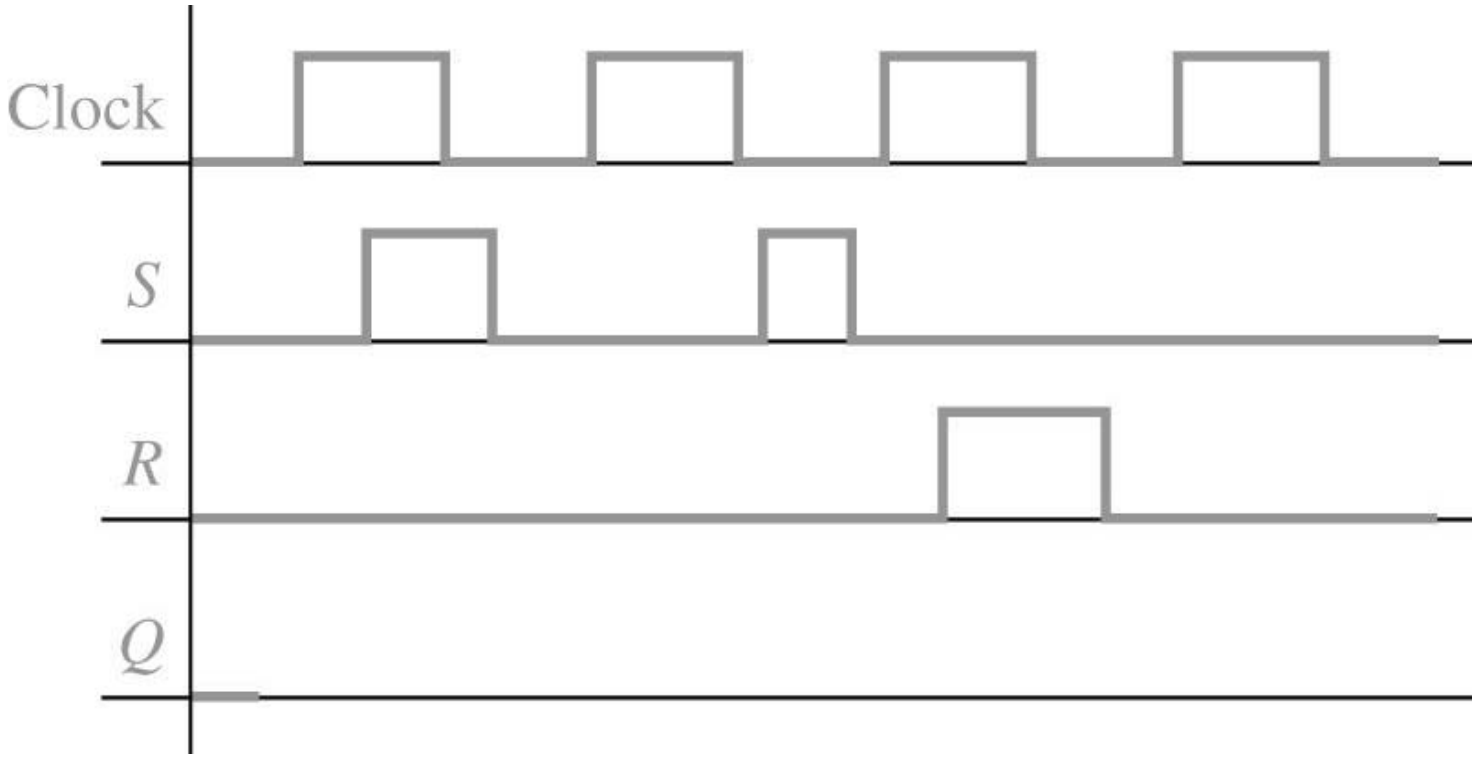


Problem 11.12

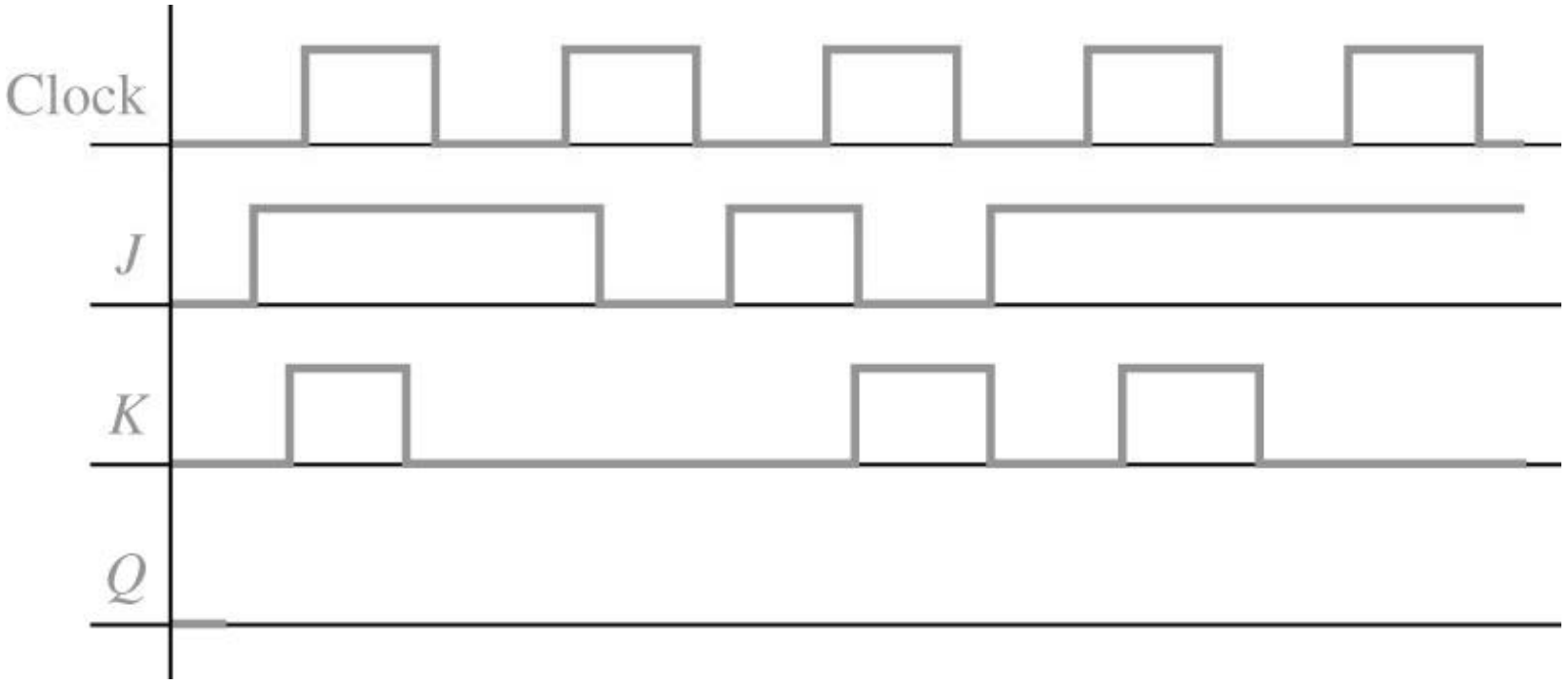
Problem 11.13



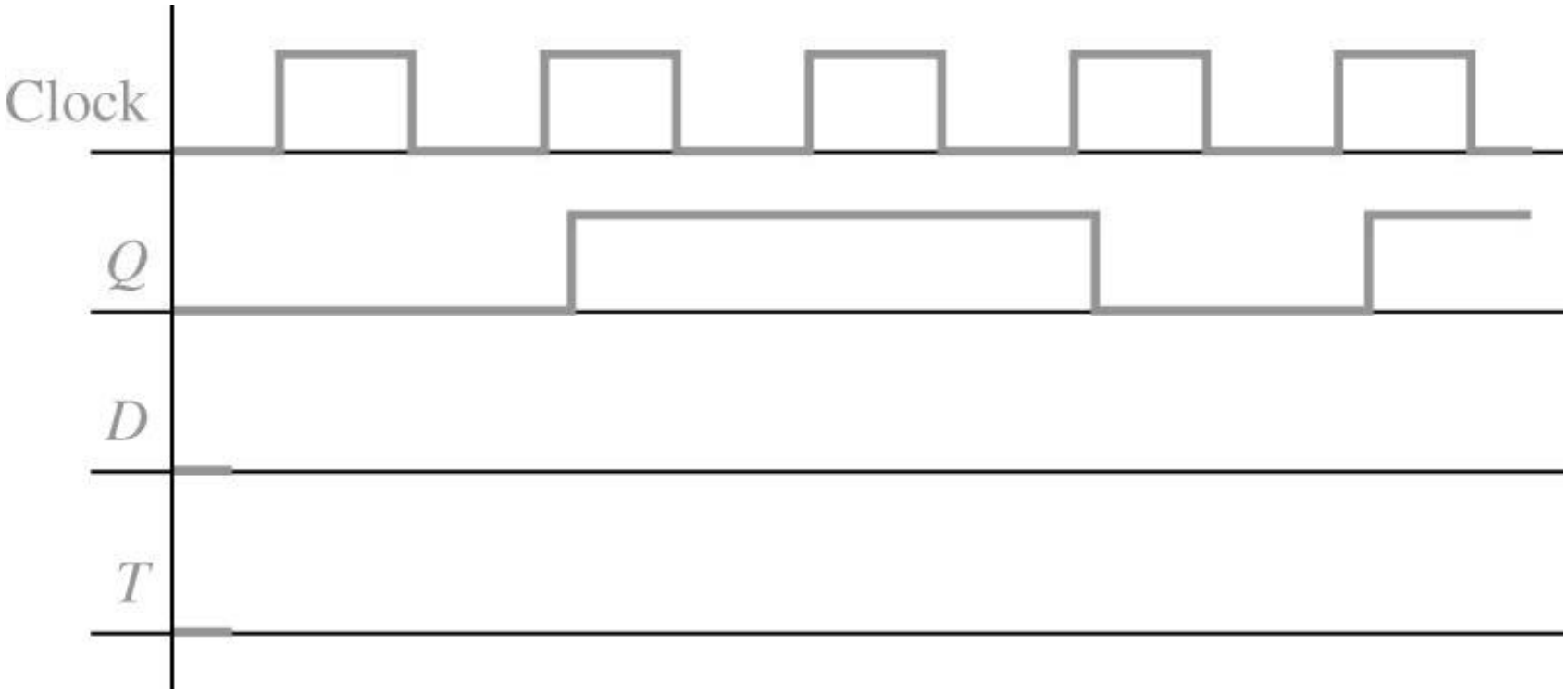
Problem 11.14



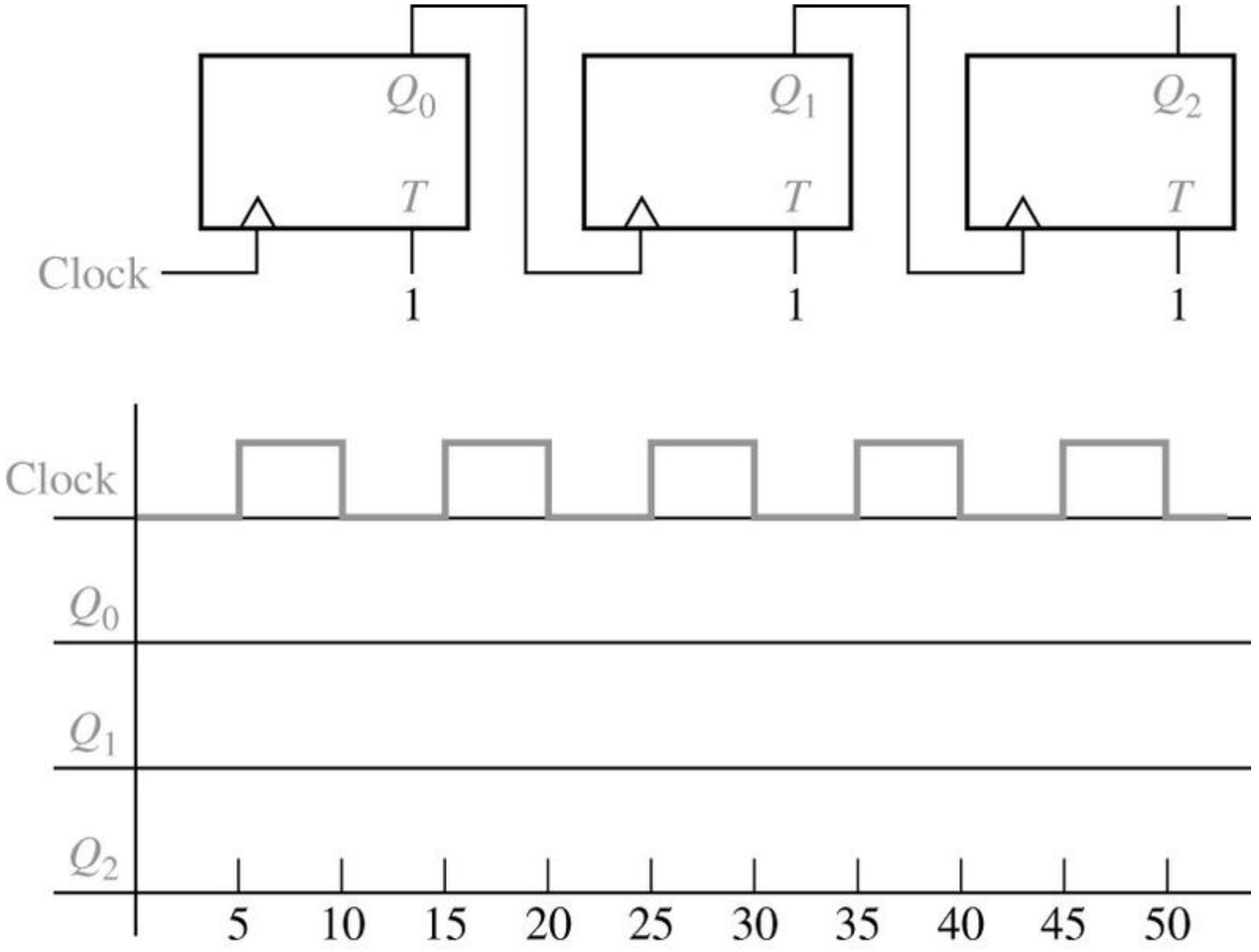
Problem 11.16



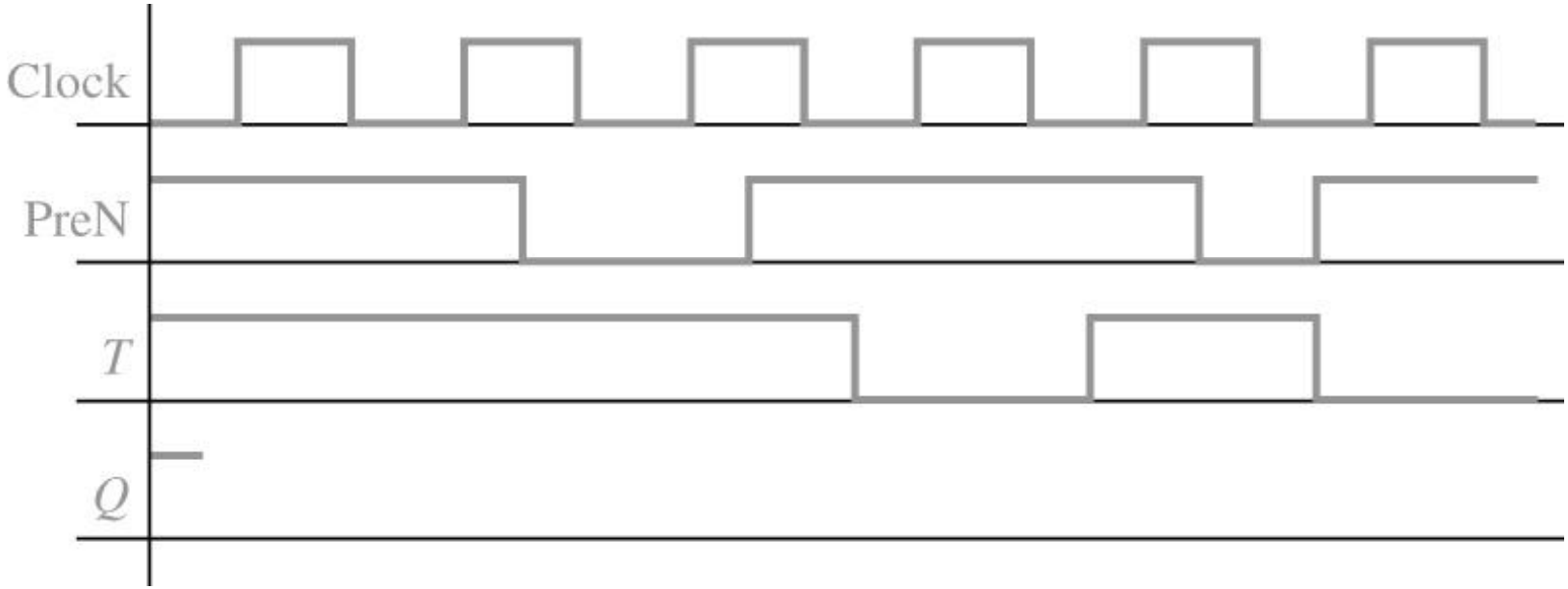
Problem 11.17



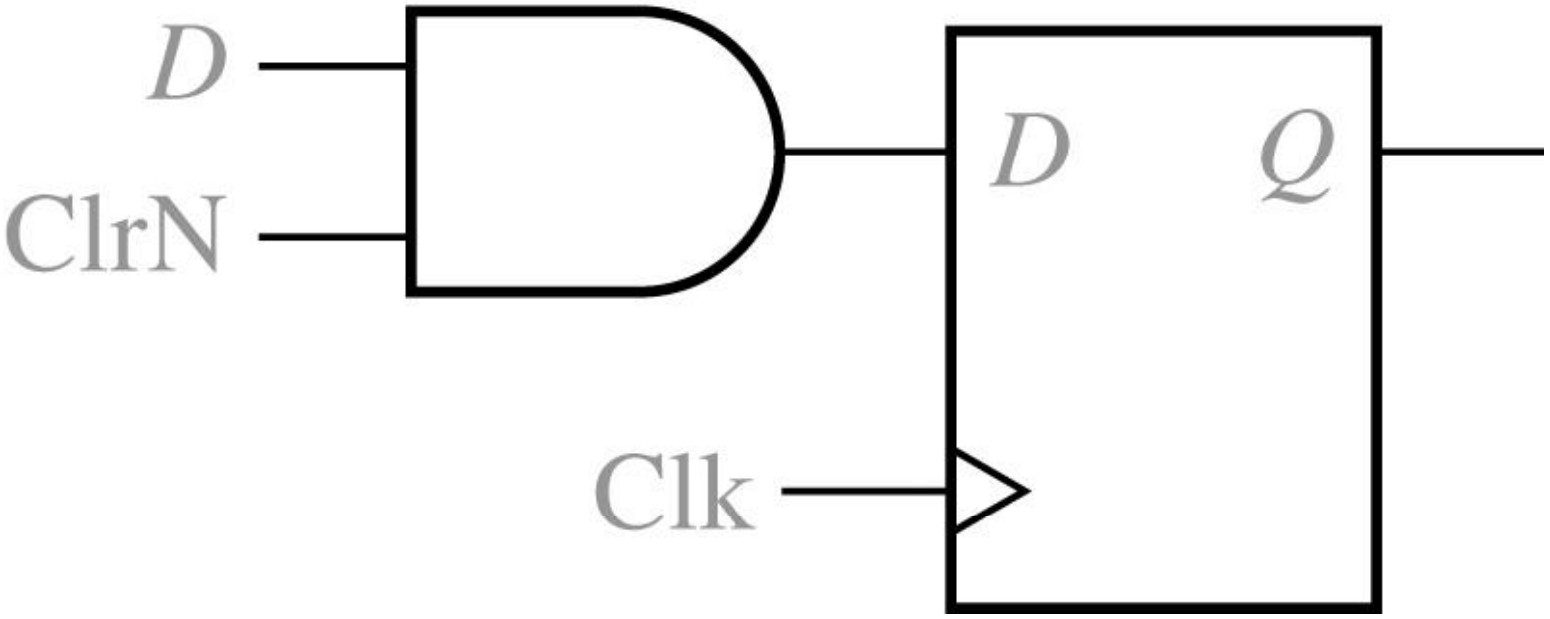
Problem 11.18



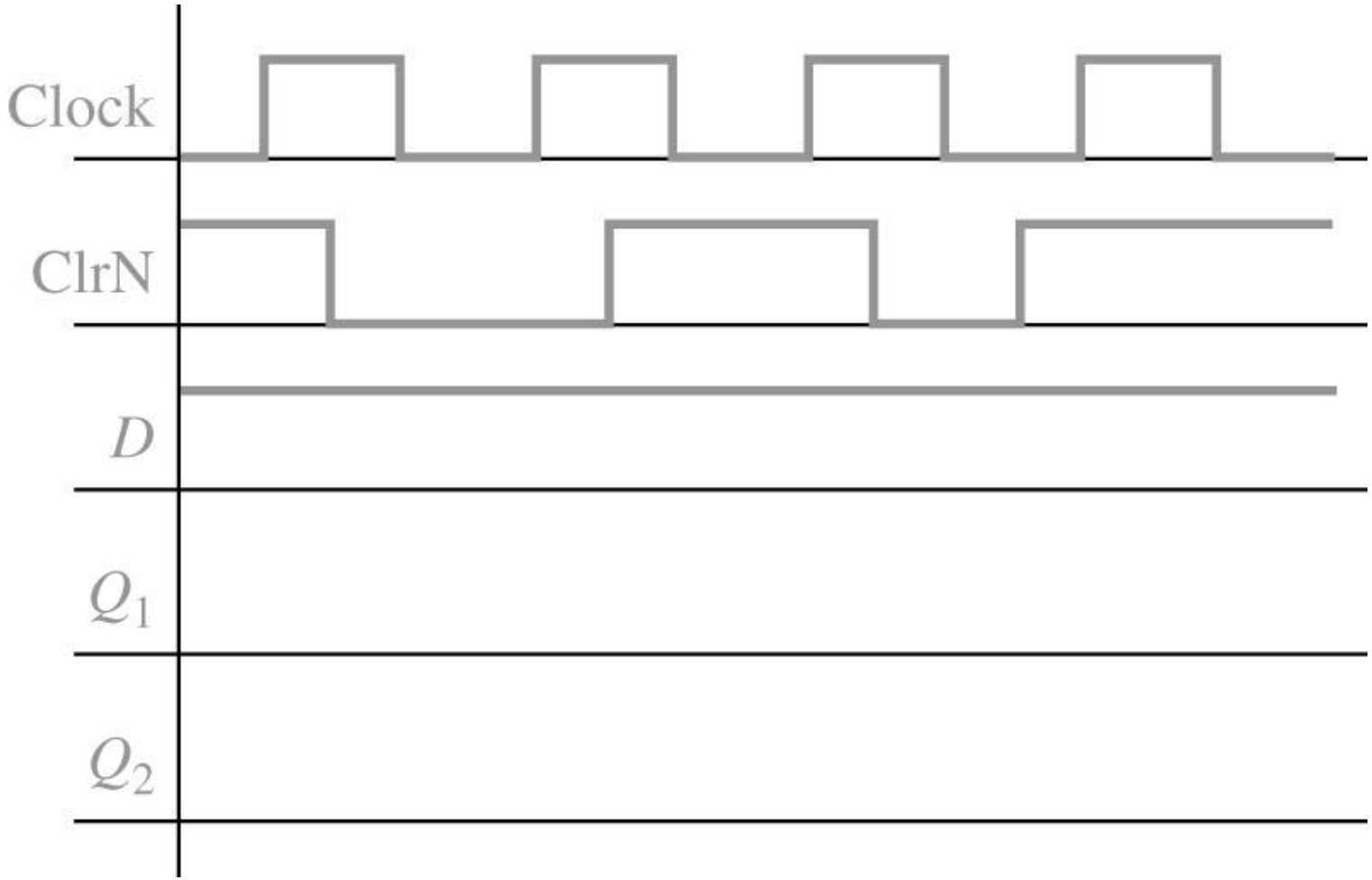
Problem 11.19



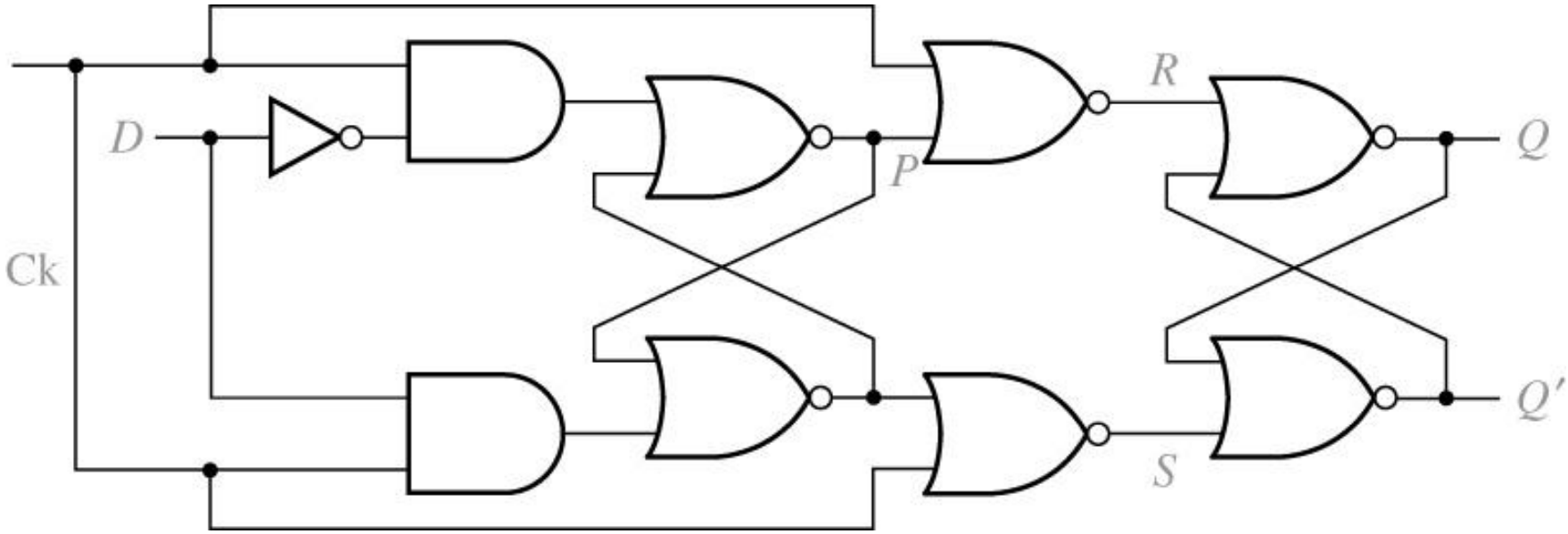
Problem 11.20



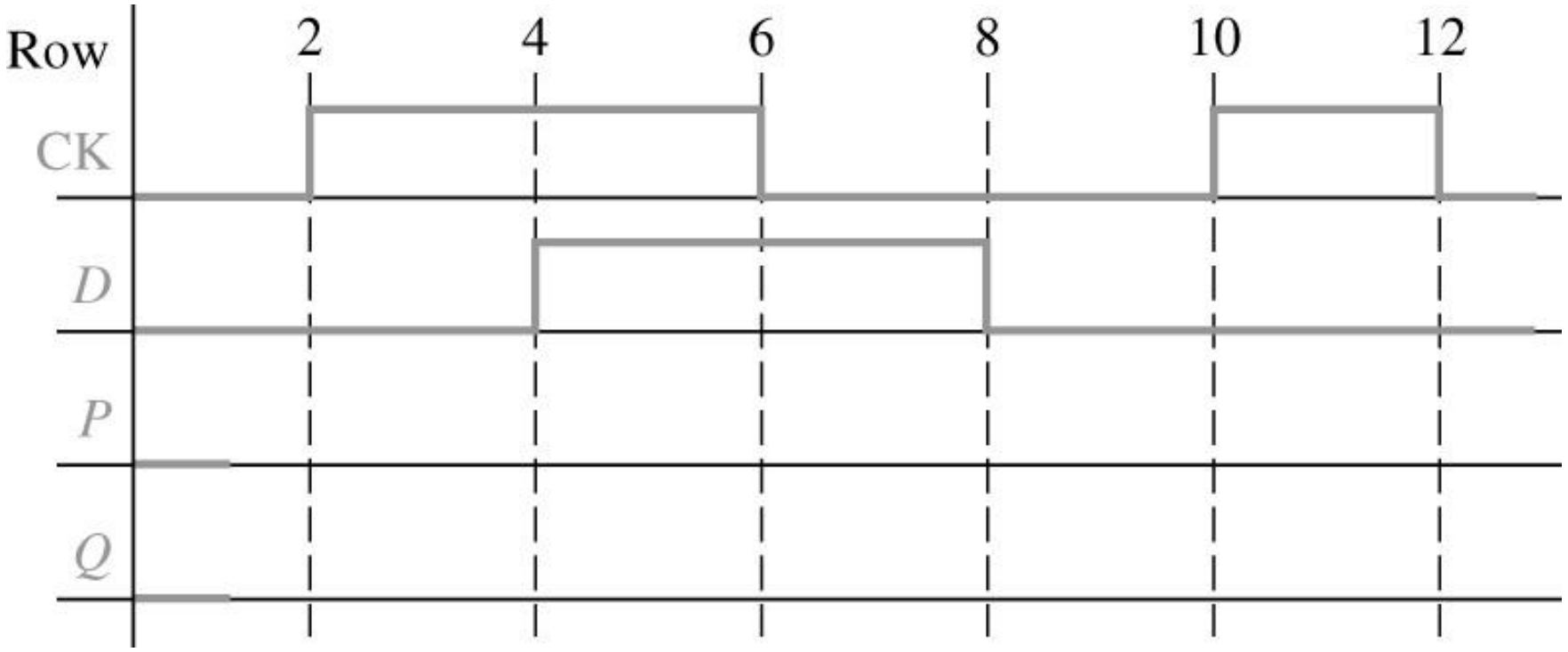
Problem 11-21 (part 1)



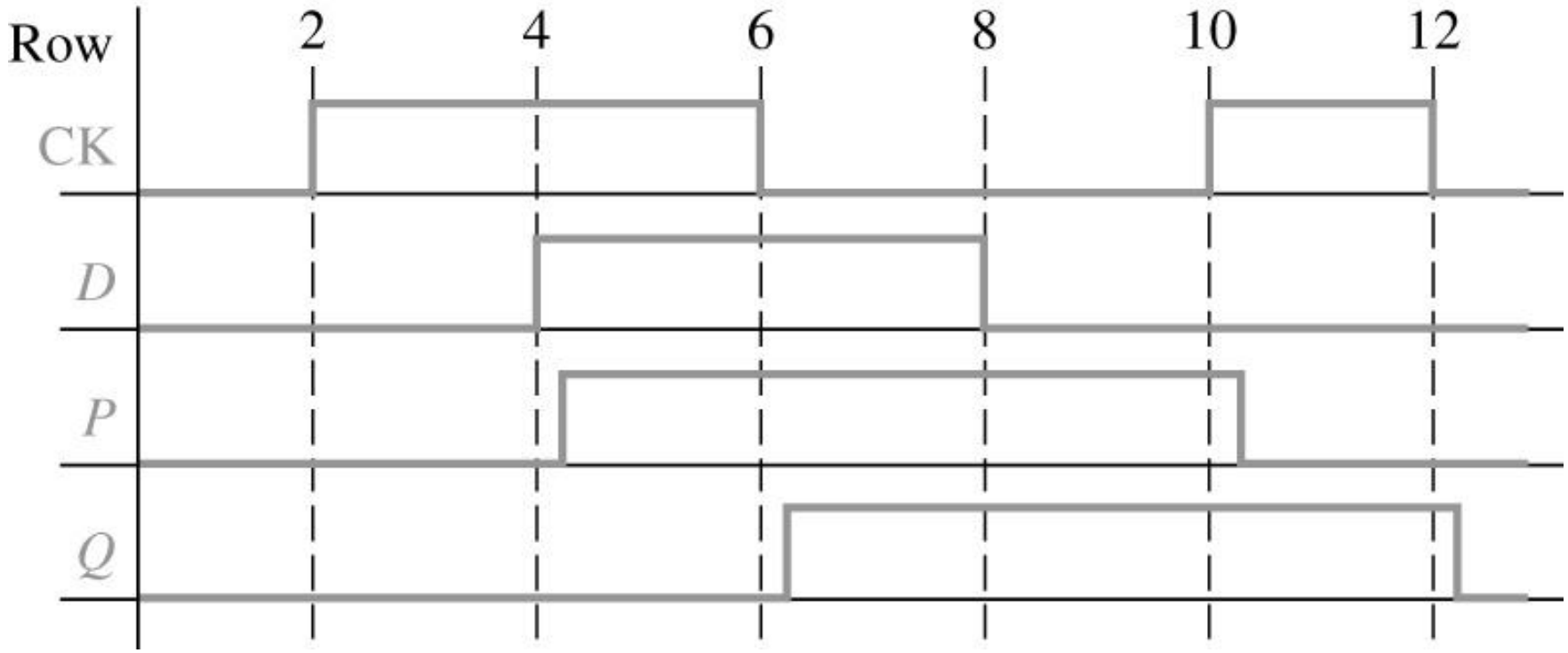
Problem 11-21 (part 2)



Programmed Exercise 11.24 (diagram)



Programmed Exercise 11.24 (Answer 5 of 6)



Programmed Exercise 11.24 (Answer 6 of 6)